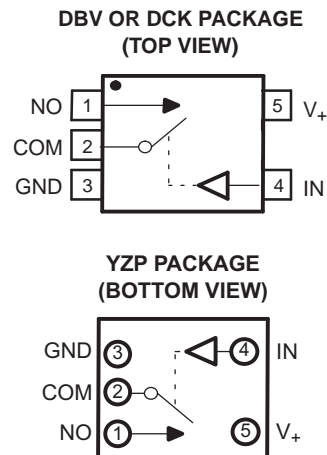


10-Ω SPST ANALOG SWITCH

Check for Samples: [TS5A1066](#)

FEATURES

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

The TS5A1066 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V₊ (peak) can be transmitted in either direction.

Table 1. SUMMARY OF CHARACTERISTICS

Configuration	Single-Pole, Single-Throw Demultiplexer (1 × SPST)
Number of channels	1
ON-state resistance (r _{on})	7.5 Ω
ON-state resistance flatness (r _{on(flat)})	2.5 Ω
Turn-on/turn-off time (t _{ON} /t _{OFF})	9.5 ns/2 ns
Charge injection (Q _C)	1 pC
Bandwidth (BW)	400 MHz
OFF isolation (O _{ISO})	–68 dB at 10 MHz
Total harmonic distortion (THD)	0.14%
Leakage current (I _{COM(OFF)})	±0.1 μA
Power-supply current (I ₊)	0.05 μA
Package options	5-pin DSBGA, SOT-23, or SC-70



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 2. ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A1066YZPR	JD_
	SOT (SOT-23) – DBV	Tape and reel	TS5A1066DBVR	JAD_
	SOT (SC-70) – DCK	Tape and reel	TS5A1066DCKR	JD_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

Absolute Minimum and Maximum Rating^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V ₊	Supply voltage range ⁽³⁾	-0.5	6.5	V
V _{NO} V _{COM}	Analog voltage range ^{(3) (4) (5)}	-0.5	V ₊ + 0.5	V
I _K	Analog port diode current V _{NO} , V _{COM} < 0 or V _{NO} , V _{COM} > V ₊	-50	50	mA
I _{NO} I _{COM}	On-state switch current V _{NO} , V _{COM} = 0 to V ₊	-50	50	mA
V _I	Digital input voltage range ^{(3) (4)}	-0.5	6.5	V
I _{IK}	Digital input clamp current V _I < 0	-50		mA
I ₊ I _{GND}	Continuous current through each V ₊ or GND	-100	100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DBV package	206	°C/W
		DCK package	252	
		YZP package	132	
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply⁽¹⁾
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -30\text{ mA}$, Switch ON, See Figure 13	25°C Full	4.5 V		7.5	10 12	Ω
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -30\text{ mA}$, Switch ON, See Figure 13	25°C Full	4.5 V		2.5	5 6	Ω
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = 4.5\text{ V}$, or $V_{NO} = 4.5\text{ V}$, $V_{COM} = 1\text{ V}$, Switch OFF, See Figure 14	25°C Full	5.5 V	-0.2 -2	0.1	0.2 2	μA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = 4.5\text{ V}$, or $V_{COM} = 4.5\text{ V}$, $V_{NO} = 1\text{ V}$, Switch OFF, See Figure 14	25°C Full	5.5 V	-0.1 -0.2	0.05	0.1 0.2	μA
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 4.5\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, See Figure 15	25°C Full	5.5 V	-0.2 -2	0.1	0.2 2	μA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 4.5\text{ V}$, $V_{NO} = \text{Open}$, Switch ON, See Figure 15	25°C Full	5.5 V	-0.1 -0.2	0.05	0.1 0.2	μA
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}		Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C Full	5.5 V	-0.1 -1	0.05	0.1 1	μA

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 5-V Supply⁽¹⁾ (continued) $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = 3\text{ V}$, $R_L = 300\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	5 V	3.5	4.8	5.5	ns
				Full	4.5 V to 5.5 V	3.5		7.5	
Turn-off time	t_{OFF}	$V_{COM} = 3\text{ V}$, $R_L = 300\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	5 V	2	3	4.5	ns
				Full	4.5 V to 5.5 V	2		5.5	
Charge injection	Q_C	$V_{GEN} = 0$, $C_L = 0.1\text{ nF}$,	See Figure 20	25°C	5 V	1		pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V	6.8		pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V	6.8		pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V	14		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V	14		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V	2.2		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	5 V	400		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, See Figure 19	25°C	5 V	-68		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 21	25°C	5 V	0.14		%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V	0.05	1	μA	
				Full			5		

Electrical Characteristics for 3.3-V Supply⁽¹⁾
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, See Figure 13	25°C Full	3 V		11.5	14	Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, See Figure 13	25°C Full	3 V		5	10	Ω
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = 3\text{ V}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = 1\text{ V}$, Switch OFF, See Figure 14	25°C Full	3.6 V	-0.2	0.1	0.2	μA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = 3\text{ V}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = 1\text{ V}$, Switch OFF, See Figure 14	25°C Full	3.6 V	-0.1	0.05	0.1	μA
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, See Figure 15	25°C Full	3.6 V	-0.2	0.1	0.2	μA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = \text{Open}$, Switch ON, See Figure 15	25°C Full	3.6 V	-0.1	0.05	0.1	μA
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}		Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C Full	3.6 V	-0.1	0.05	0.1	μA
					-1		1	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 3.3-V Supply⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	3.3 V	4.5	5.5	8	ns
				Full	3 V to 3.6 V	4.5		8.5	
Turn-off time	t_{OFF}	$V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	3.3 V	2	3	4.5	ns
				Full	3 V to 3.6 V	2		5.5	
Charge injection	Q_C	$V_{GEN} = 0$, $C_L = 0.1\text{ nF}$,	See Figure 20	25°C	3.3 V	1		pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V	6.8		pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V	6.8		pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V	14		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V	14		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V	2.2		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	3.3 V	400		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, See Figure 19	25°C	3.3 V	-68		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 21	25°C	3.3 V	0.2		%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	0.05	1	μA	
				Full			5		

Electrical Characteristics for 2.5-V Supply⁽¹⁾
 $V_+ = 2.3\text{ V to }2.7\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -8\text{ mA}$, Switch ON, See Figure 13	25°C	2.3 V	20		24	Ω
			Full				27	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -8\text{ mA}$, Switch ON, See Figure 13	25°C	2.3 V	7.5		15	Ω
			Full				20	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0.5\text{ V}$, $V_{COM} = 2.2\text{ V}$, or $V_{NO} = 2.2\text{ V}$, $V_{COM} = 0.5\text{ V}$, Switch OFF, See Figure 14	25°C	2.7 V	-0.2	0.1	0.2	μA
			Full		-2		2	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0.5\text{ V}$, $V_{NO} = 2.2\text{ V}$, or $V_{COM} = 2.2\text{ V}$, $V_{NO} = 0.5\text{ V}$, Switch OFF, See Figure 14	25°C	2.7 V	-0.1	0.05	0.1	μA
			Full		-0.2		0.2	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.5\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 2.2\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, See Figure 15	25°C	2.7 V	-0.2	0.1	0.2	μA
			Full		-2		2	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.5\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 2.2\text{ V}$, $V_{NO} = \text{Open}$, Switch ON, See Figure 15	25°C	2.7 V	-0.1	0.05	0.1	μA
			Full		-0.2		0.2	
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}		Full		0	$V_+ \times 0.3$		V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C	2.7 V	-0.1	0.05	0.1	μA
			Full		-1		1	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued)
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t_{ON}	$V_{COM} = 1.5 \text{ V}$, $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, See Figure 17	25°C	2.5 V	4.5	5.5	8	ns
			Full	2.3 V to 2.7 V	4.5		8.5	
Turn-off time	t_{OFF}	$V_{COM} = 1.5 \text{ V}$, $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, See Figure 17	25°C	2.5 V	1.5	2.5	4	ns
			Full	2.3 V to 2.7 V	1.5		5.5	
Charge injection	Q_C	$V_{GEN} = 0$, $C_L = 0.1 \text{ nF}$, See Figure 20	25°C	2.5 V		1		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		6.8		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		6.8		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		14		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V		2.2		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON, See Figure 18	25°C	2.5 V		400		MHz
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch OFF, See Figure 19	25°C	2.5 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 21	25°C	2.5 V		0.32		%
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V		0.05	1	μA
			Full					

Electrical Characteristics for 1.8-V Supply⁽¹⁾
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -4\text{ mA}$, Switch ON, See Figure 13	25°C	1.65 V	74.5		80	Ω
			Full				100	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -4\text{ mA}$, Switch ON, See Figure 13	25°C	1.65 V	64.5		70	Ω
			Full				90	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0.3\text{ V}$, $V_{COM} = 1.65\text{ V}$, or $V_{NO} = 1.65\text{ V}$, $V_{COM} = 0.3\text{ V}$, Switch OFF, See Figure 14	25°C	1.95 V	-0.2	0.1	0.2	μA
			Full		-2		2	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0.3\text{ V}$, $V_{NO} = 1.65\text{ V}$, or $V_{COM} = 1.65\text{ V}$, $V_{NO} = 0.3\text{ V}$, Switch OFF, See Figure 14	25°C	1.95 V	-0.1	0.05	0.1	μA
			Full		-0.2		0.2	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.3\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 1.65\text{ V}$, $V_{COM} = \text{Open}$, Switch ON, See Figure 15	25°C	1.95 V	-0.2	0.1	0.2	μA
			Full		-2		2	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.3\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 1.65\text{ V}$, $V_{NO} = \text{Open}$, Switch ON, See Figure 15	25°C	1.95 V	-0.1	0.05	0.1	μA
			Full		-0.2		0.2	
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		$V_+ \times 0.65$		5.5	V
Input logic low	V_{IL}		Full		0	$V_+ \times 0.35$		V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$	25°C	1.95 V	-0.1	0.05	0.1	μA
			Full		-1		1	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 1.8-V Supply⁽¹⁾ (continued)
 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = 1.3 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 17	25°C	1.8 V	9.5	10	12	ns
				Full	1.65 V to 1.95 V	8.5		13	
Turn-off time	t_{OFF}	$V_{COM} = 1.3 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 17	25°C	1.8 V	1.5	2	4	ns
				Full	1.65 V to 1.95 V	1.5		5.5	
Charge injection	Q_C	$V_{GEN} = 0$, $C_L = 0.1 \text{ nF}$,	See Figure 20	25°C	1.8 V		1		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6.8		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6.8		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14		pF
Digital input capacitance	C_i	$V_i = V_+$ or GND,	See Figure 16	25°C	1.8 V		2.2		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	1.8 V		400		MHz
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$,	Switch OFF, See Figure 19	25°C	1.8 V		-68		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 21	25°C	1.8 V		0.32		%
Supply									
Positive supply current	I_+	$V_i = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.05	1	μA
				Full				5	

TYPICAL PERFORMANCE

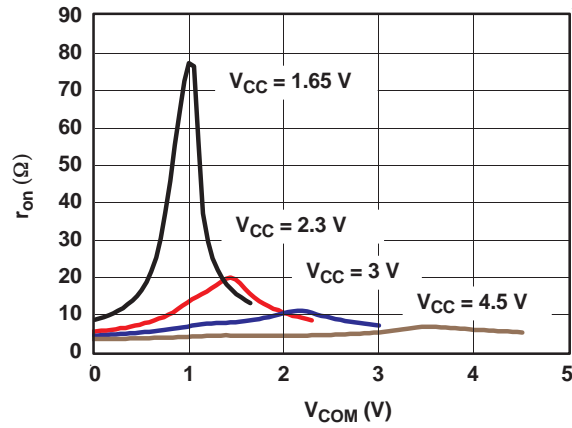


Figure 1. r_{on} vs V_{COM}

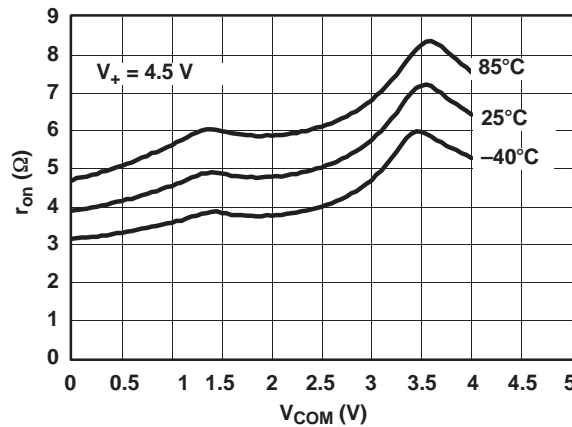


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

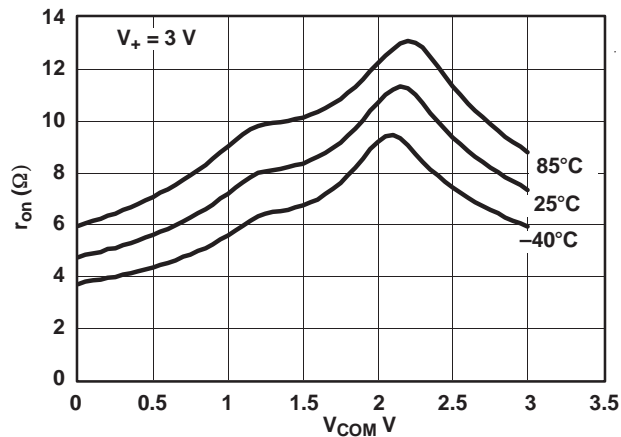


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

TYPICAL PERFORMANCE

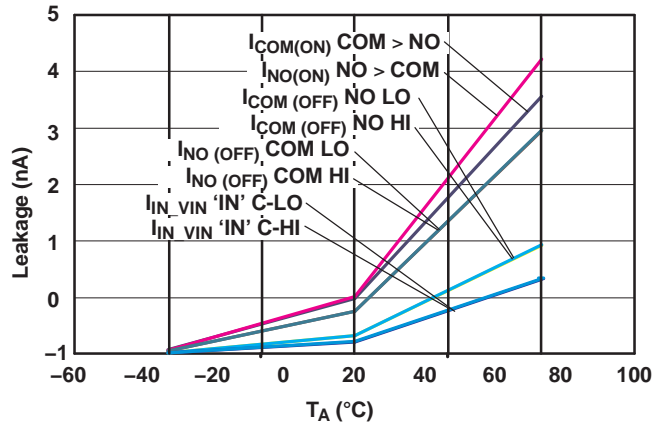


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5\text{ V}$)

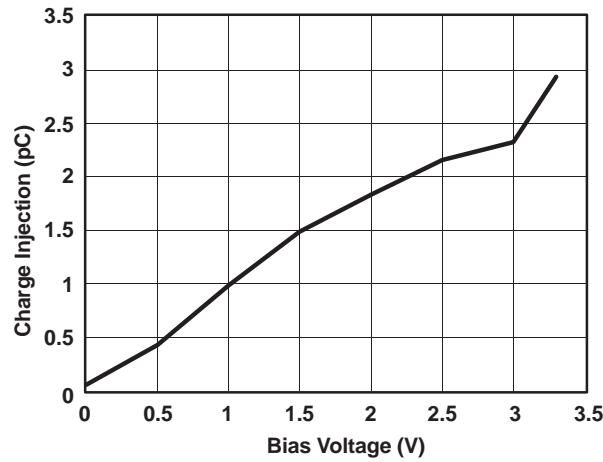


Figure 5. Charge Injection (Q_C) vs Bias Voltage

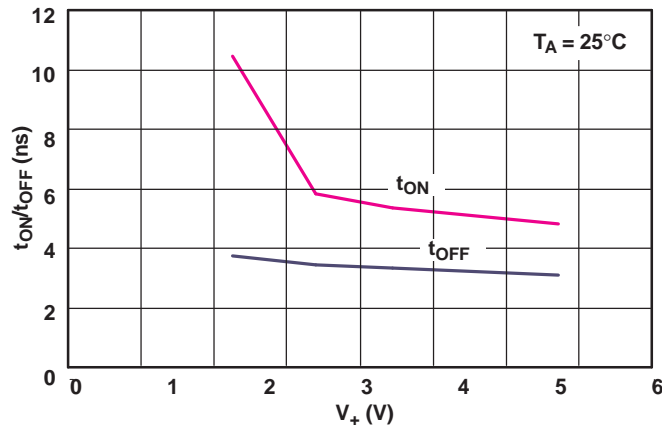


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE

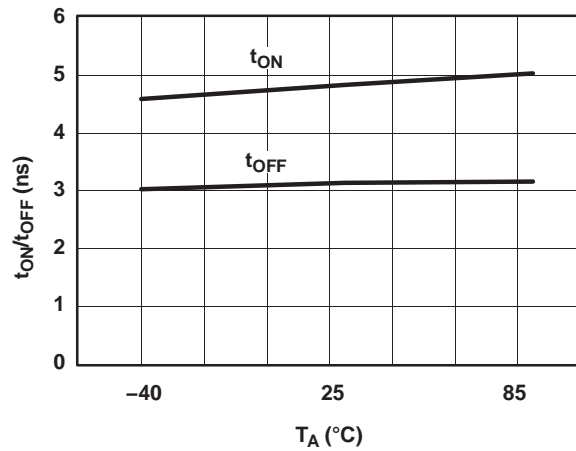


Figure 7. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5$ V)

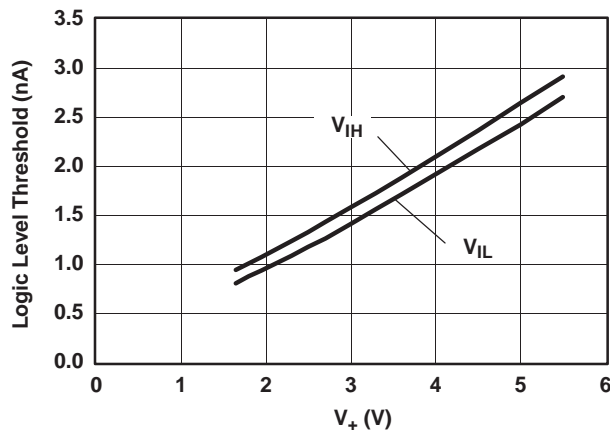


Figure 8. Logic-Level Threshold vs V_+

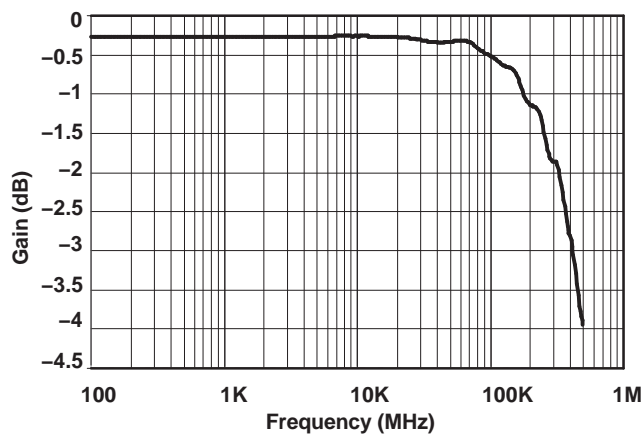


Figure 9. Bandwidth ($V_+ = 5$ V)

TYPICAL PERFORMANCE

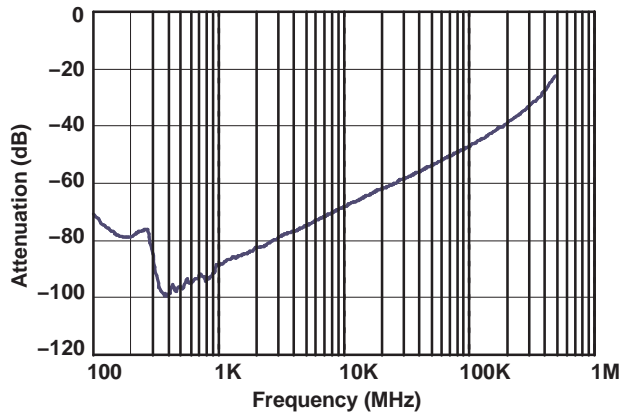


Figure 10. OFF Isolation ($V_+ = 5\text{ V}$)

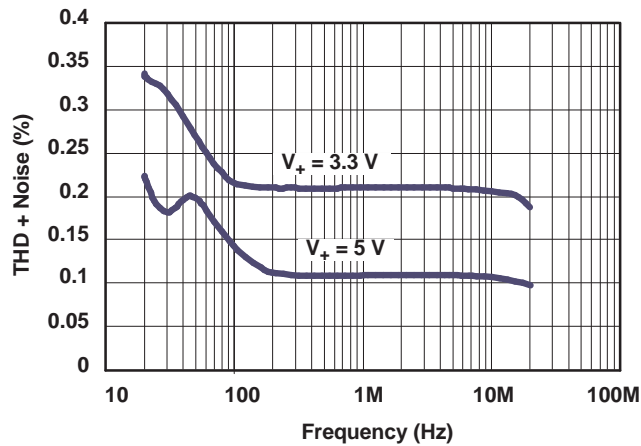


Figure 11. Total Harmonic Distortion vs Frequency

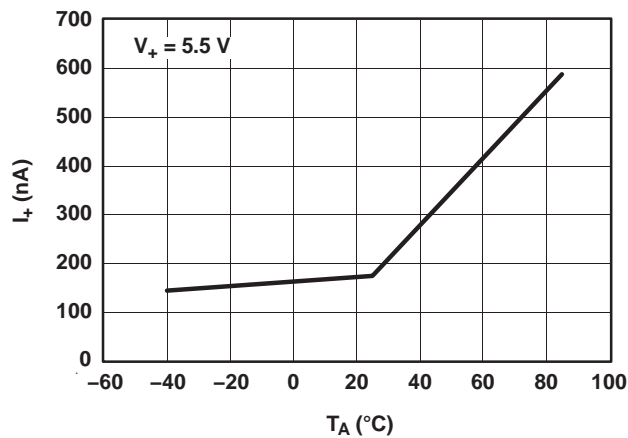


Figure 12. Power-Supply Current vs Temperature ($V_+ = 5\text{ V}$)

Table 3. PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	NO	Normally open
2	COM	Common
3	GND	Digital ground
4	IN	Digital control to connect COM to NO
5	V ₊	Power supply

Table 4. PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NO ports when the channel is ON
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I _{COM(OFF)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Maximum input voltage for logic low for the control input (IN)
V _I	Voltage at the control input (IN)
I _{IH} , I _{IL}	Leakage current measured at the control input (IN)
t _{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t _{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _{COM} , C _L is the load capacitance and ΔV _{COM} is the change in analog output voltage.
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(OFF)}	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C _I	Capacitance of IN
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I ₊	Static power-supply current with the control (IN) pin at V ₊ or GND
ΔI ₊	This is the increase in I ₊ for each control (IN) input that is at the specified voltage, rather than at V ₊ or GND.

PARAMETER MEASUREMENT INFORMATION

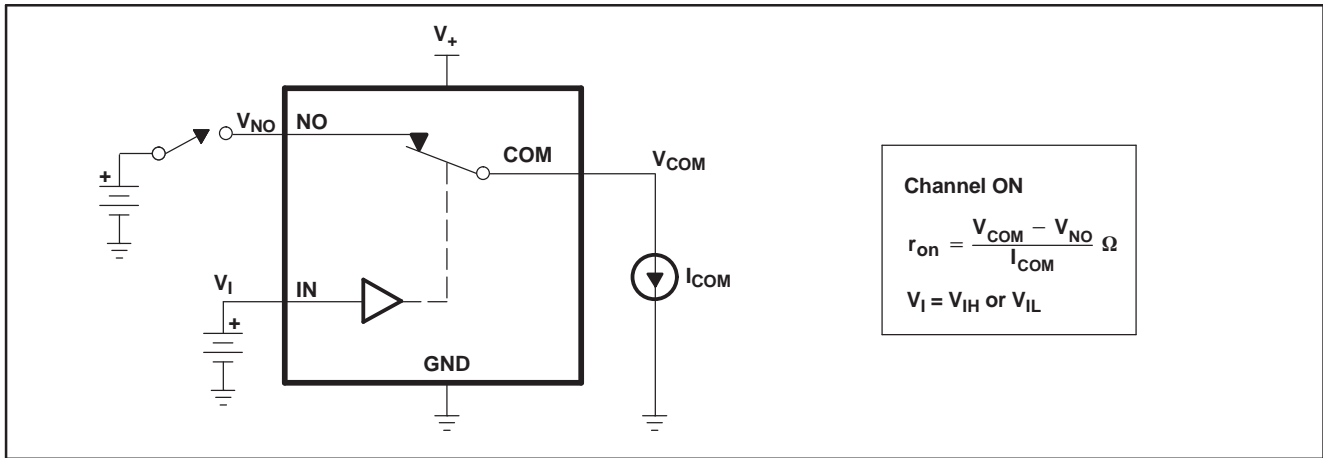


Figure 13. ON-State Resistance (r_{on})

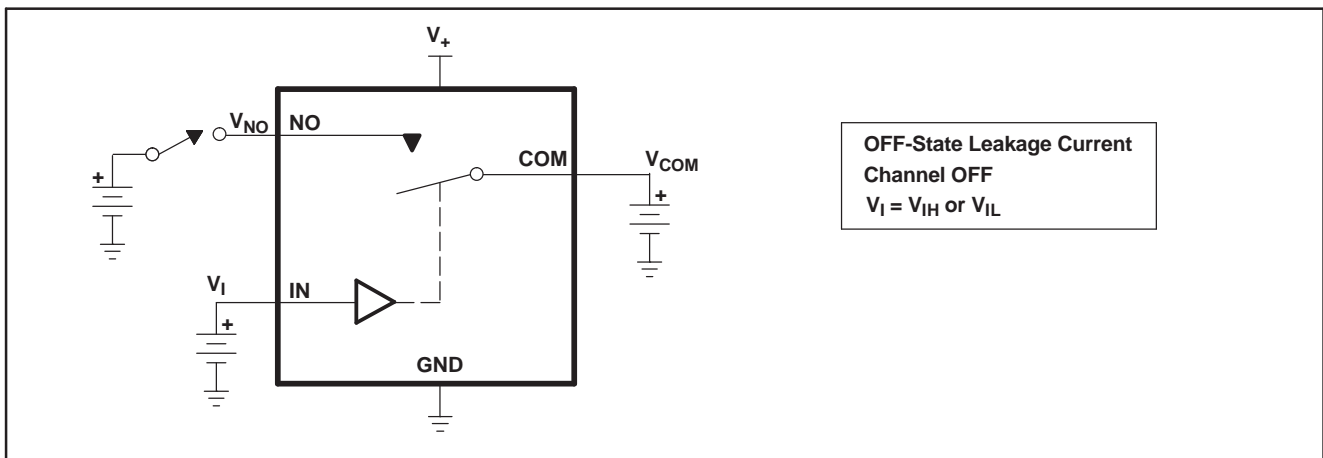


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

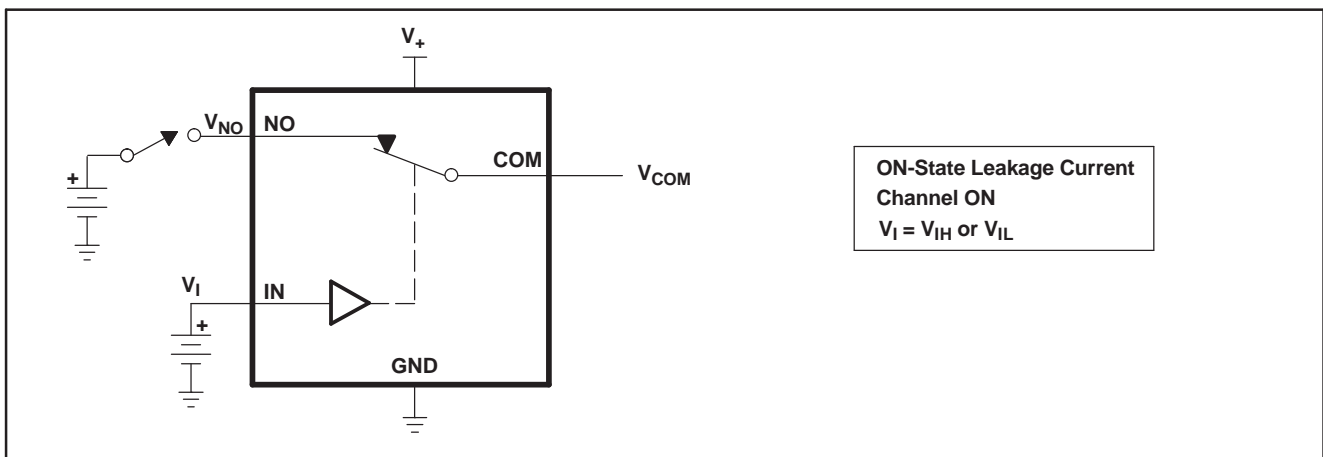


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

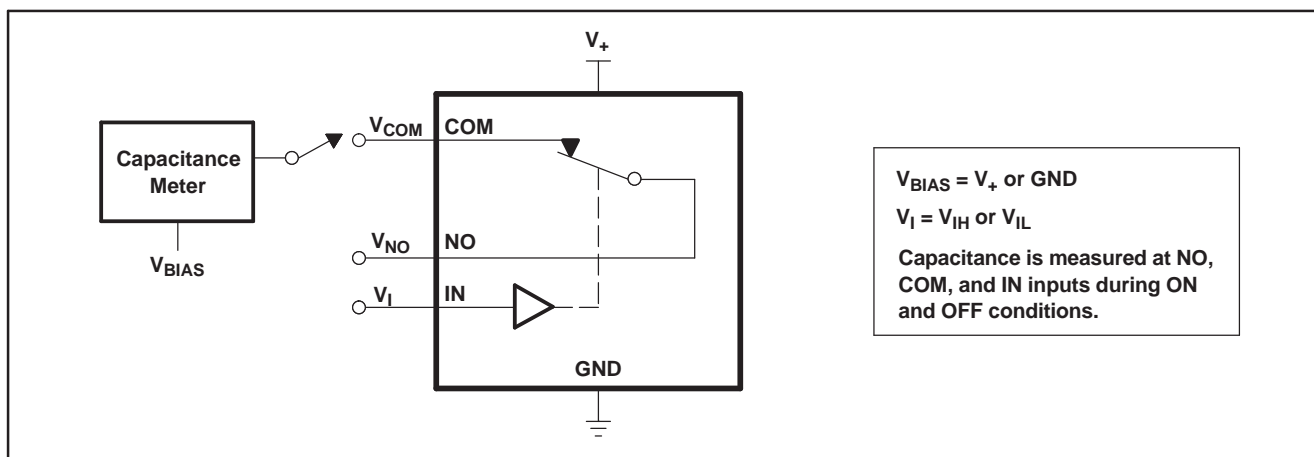
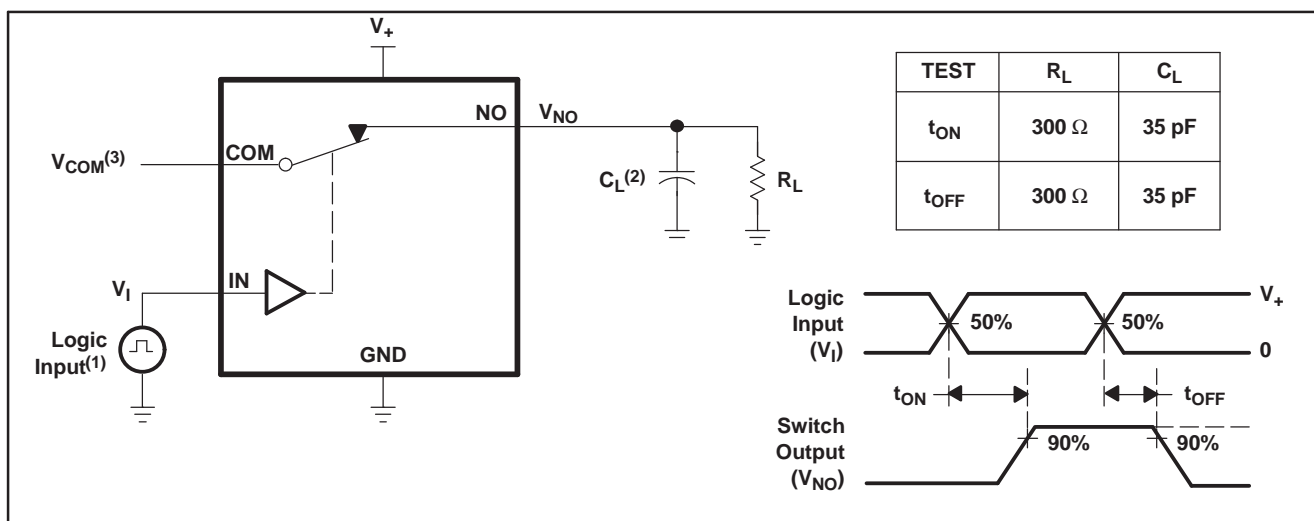


Figure 16. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- (2) C_L includes probe and jig capacitance.
- (3) See Electrical Characteristics for V_{COM} .

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)

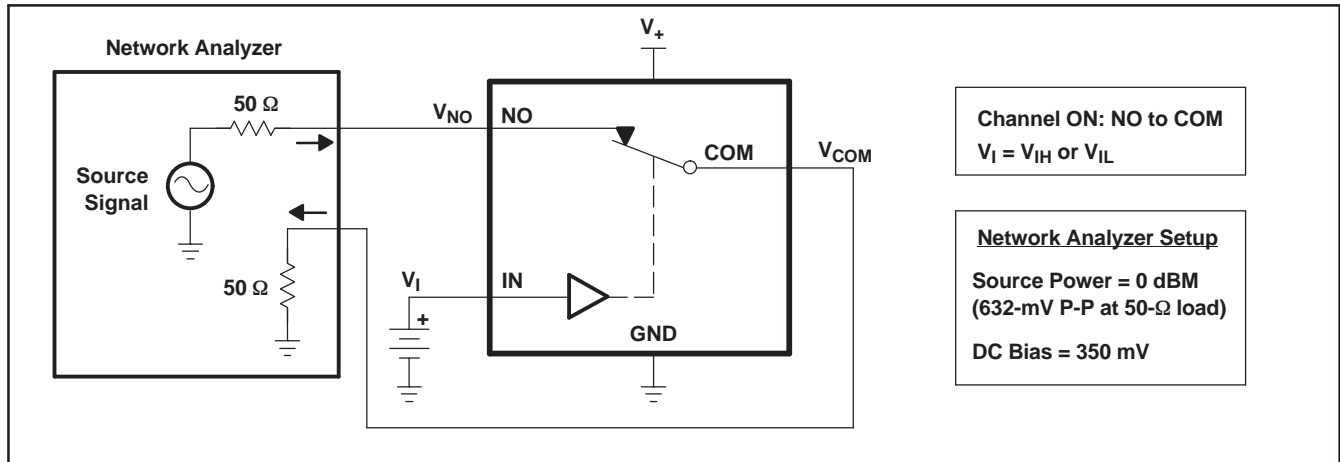


Figure 18. Bandwidth (BW)

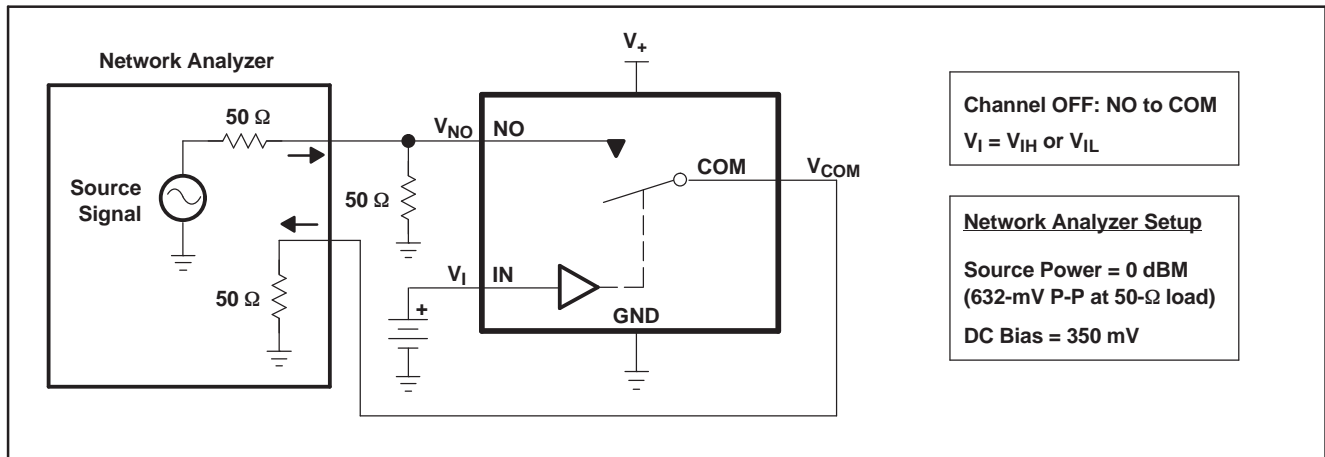
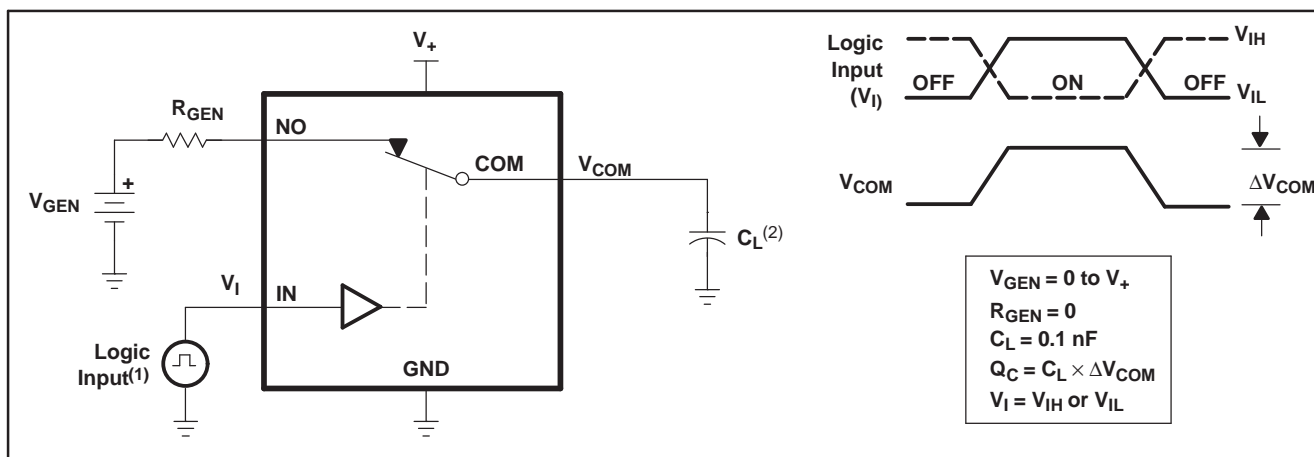


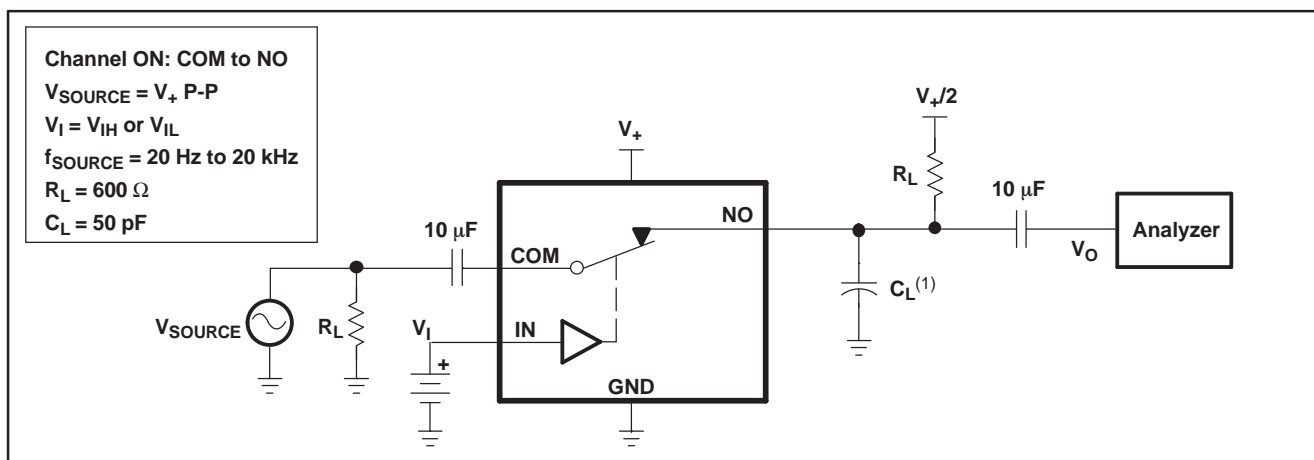
Figure 19. OFF Isolation (O_{ISO})

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.

Figure 20. Charge Injection (Q_C)



- (1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

REVISION HISTORY

Changes from Revision B (April 2006) to Revision C	Page
• Updated package options information.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A1066DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(JADF ~ JADR)	Samples
TS5A1066DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JADF	Samples
TS5A1066DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JD5 ~ JDF ~ JDR)	Samples
TS5A1066DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JD5 ~ JDF ~ JDR)	Samples
TS5A1066YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JD7 ~ JDN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A1066DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A1066DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A1066DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A1066DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A1066DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A1066YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

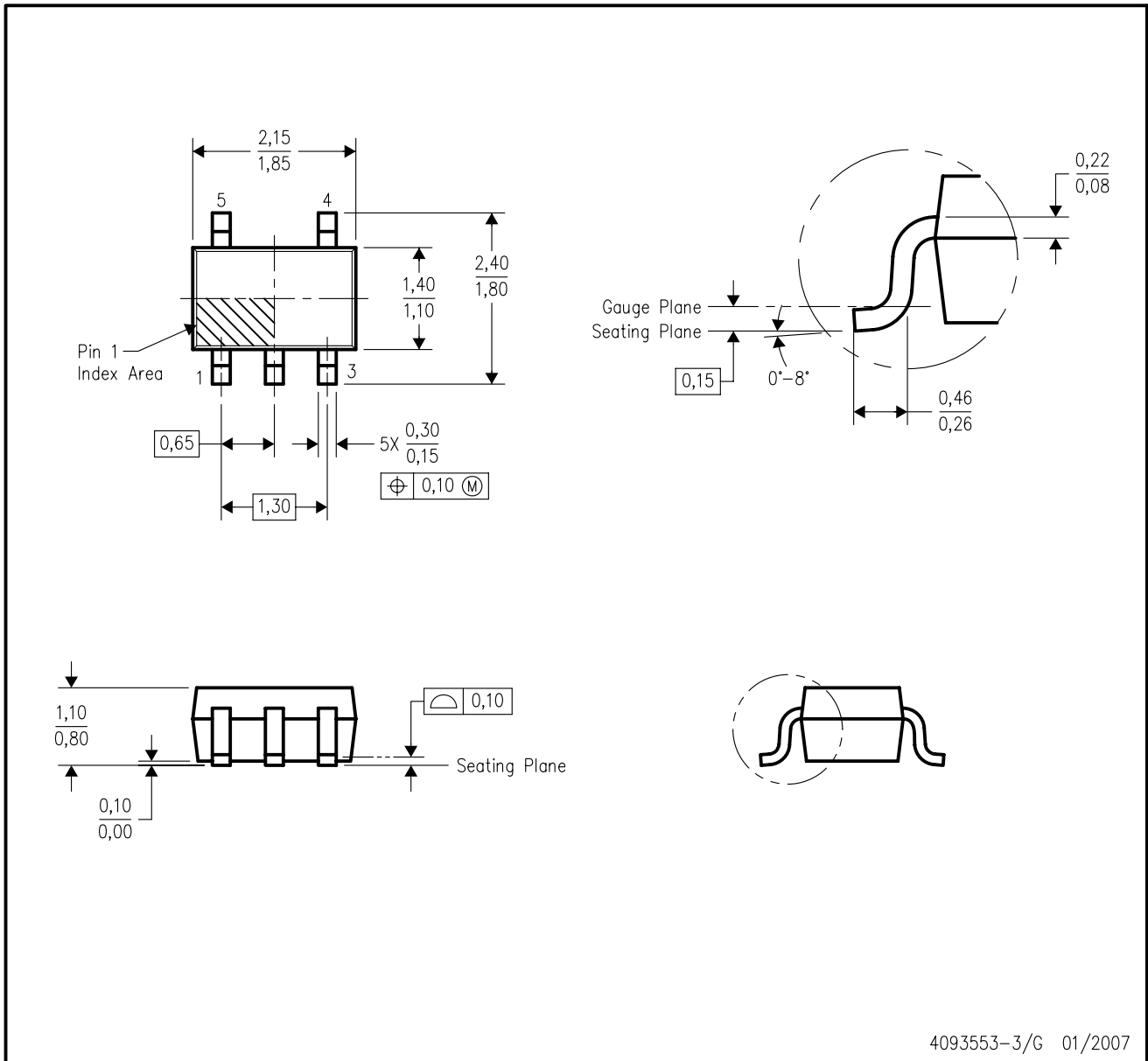
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A1066DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A1066DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A1066DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A1066DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A1066DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A1066YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

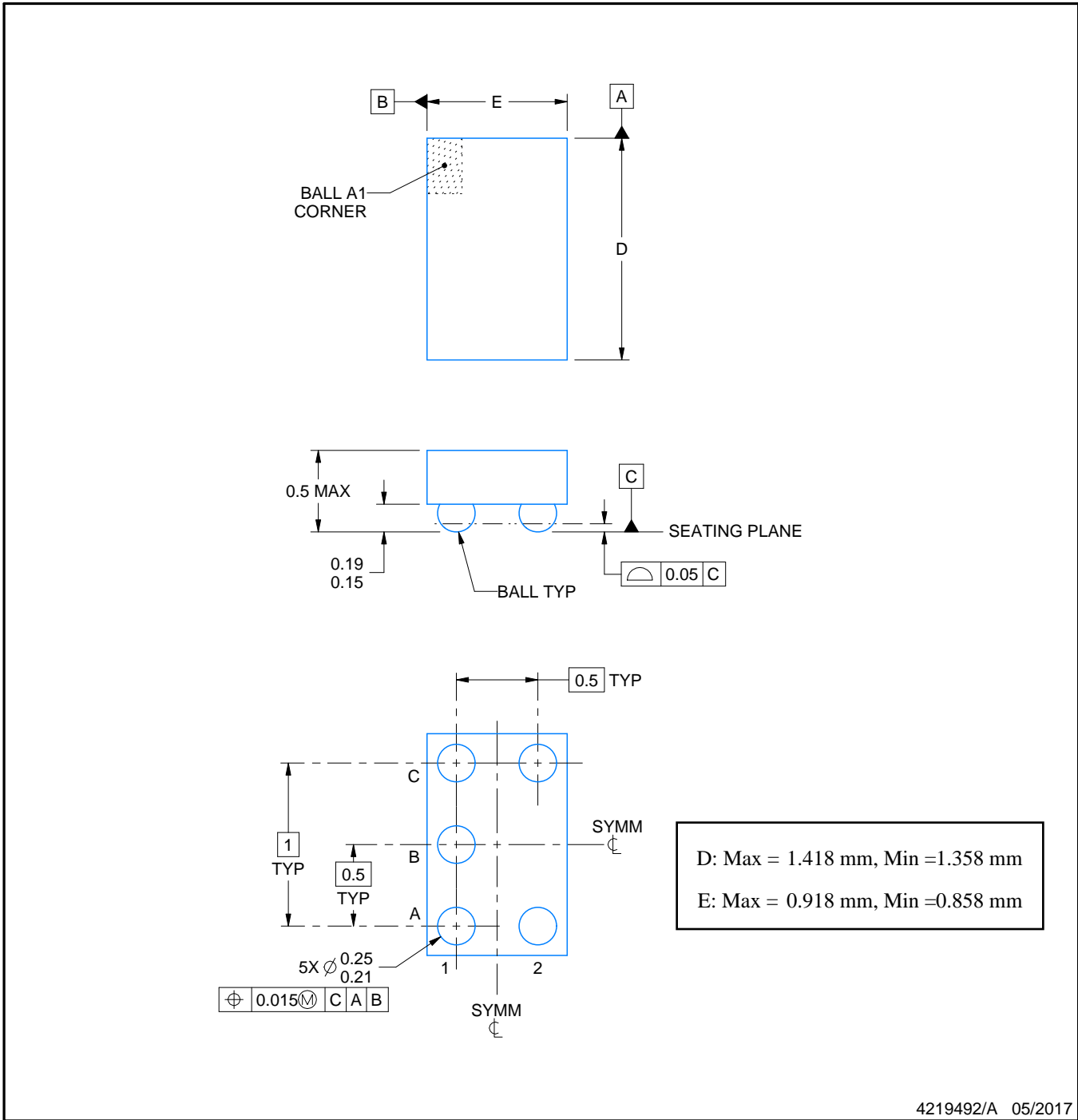
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.