

## TLC6C598-Q1 Power Logic 8-Bit Shift Register LED Driver

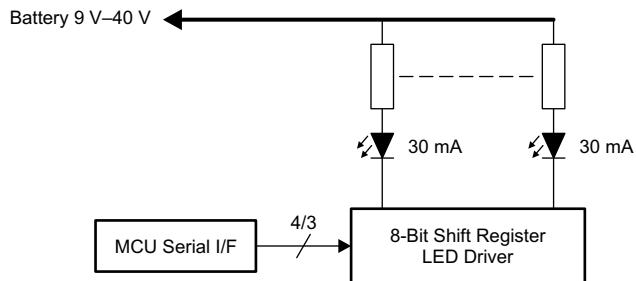
### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide  $V_{CC}$  From 3 V to 5.5 V
- Output Maximum Rating of 40 V
- Eight Power DMOS Transistor Outputs of 50-mA Continuous Current With  $V_{CC} = 5\text{ V}$
- Thermal Shutdown Protection
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption
- Slow Switching Time ( $t_r$  and  $t_f$ ), Which Helps Significantly With Reducing EMI
- 16-Pin TSSOP-PW Package
- 16-Pin SOIC-D Package

### 2 Applications

- Instrumentation Cluster
- Tell-Tale Lamps
- LED Illumination and Control

#### Typical Application Schematic



### 3 Description

The TLC6C598-Q1 is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high. A low on CLR clears all registers in the device. Holding the output enable (G) high, holds all data in the output buffers low, and all drain outputs are off. Holding  $\bar{G}$  low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50 mA continuous sink-current capabilities when  $V_{CC} = 5\text{ V}$ . The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and 200 V when using the machine model.

The TLC6C598-Q1 characterization is for for operation over the operating ambient temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)   |
|-------------|------------|-------------------|
| TLC6C598-Q1 | SOIC (16)  | 9.90 mm x 3.91 mm |
|             | TSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



## Table of Contents

|  |    |  |    |
|--|----|--|----|
| <b>1 Features</b> .....                          | 1  | 8.2 Functional Block Diagram .....                               | 11 |
| <b>2 Applications</b> .....                      | 1  | 8.3 Feature Description .....                                    | 12 |
| <b>3 Description</b> .....                       | 1  | 8.4 Device Functional Modes .....                                | 12 |
| <b>4 Revision History</b> .....                  | 2  | <b>9 Application and Implementation</b> .....                    | 13 |
| <b>5 Pin Configuration and Functions</b> .....   | 3  | 9.1 Application Information .....                                | 13 |
| <b>6 Specifications</b> .....                    | 4  | 9.2 Typical Application .....                                    | 13 |
| 6.1 Absolute Maximum Ratings .....               | 4  | <b>10 Power Supply Recommendations</b> .....                     | 16 |
| 6.2 ESD Ratings .....                            | 4  | <b>11 Layout</b> .....   | 16 |
| 6.3 Recommended Operating Conditions .....       | 4  | 11.1 Layout Guidelines .....                                     | 16 |
| 6.4 Thermal Information .....                    | 4  | 11.2 Layout Example .....  | 16 |
| 6.5 Electrical Characteristics .....             | 5  | <b>12 Device and Documentation Support</b> .....                 | 17 |
| 6.6 Timing Requirements .....                    | 5  | 12.1 Receiving Notification of Documentation Updates .....       | 17 |
| 6.7 Switching Characteristics .....              | 6  | 12.2 Community Resources .....                                   | 17 |
| 6.8 Timing Waveforms .....                       | 7  | 12.3 Trademarks .....  | 17 |
| 6.9 Typical Characteristics .....                | 8  | 12.4 Electrostatic Discharge Caution .....                       | 17 |
| <b>7 Parameter Measurement Information</b> ..... | 9  | 12.5 Glossary .....  | 17 |
| <b>8 Detailed Description</b> .....              | 11 | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | 17 |
| 8.1 Overview .....                               | 11 | 13.1 Package Option Addendum .....                               | 18 |

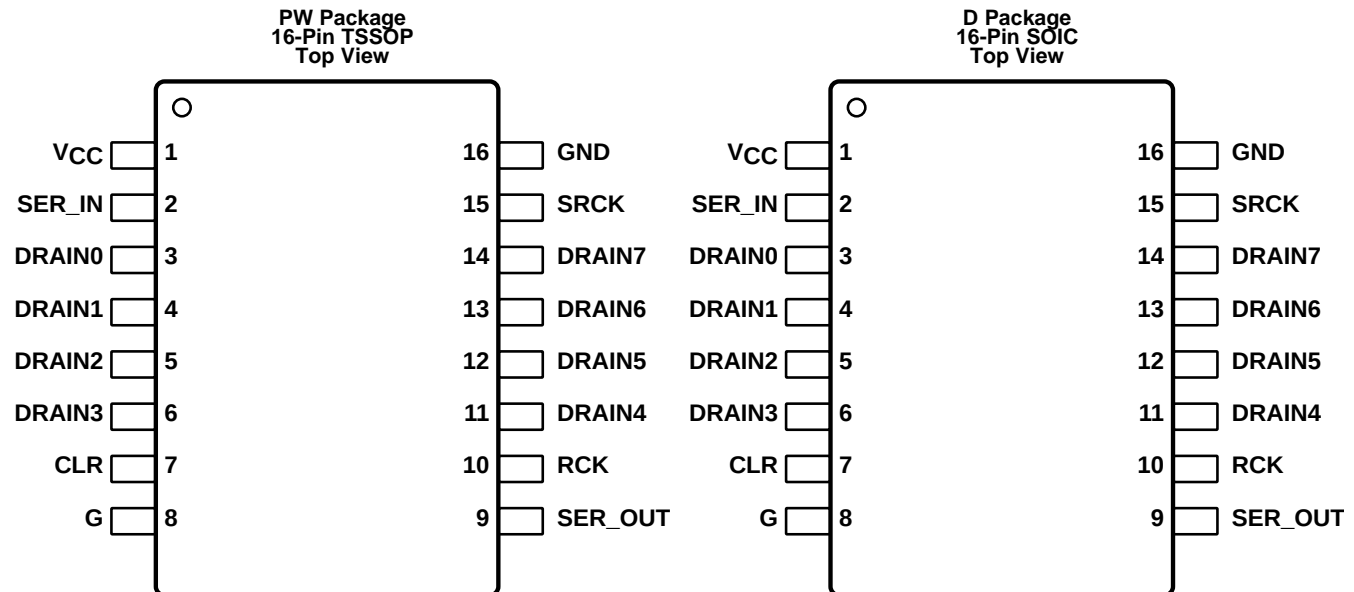
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2015) to Revision D                         | Page |
|--|------|
| • Added <i>Receiving Notification of Documentation Updates</i> section ..... | 17   |
| • Added new orderable part number to <i>Package Option Addendum</i> .....    | 18   |

| Changes from Revision B (March 2013) to Revision C   | Page |
|--|------|
| • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN                     |     | I/O | DESCRIPTION   |
|-------------------------|-----|-----|---|
| NAME                    | NO. |     |   |
| $\overline{\text{CLR}}$ | 7   | I   | Shift register clear, active-low. The storage register transfers data to the output buffer when $\overline{\text{CLR}}$ is high. Driving $\overline{\text{CLR}}$ low clears all the registers in the device.      |
| DRAIN0                  | 3   | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN1                  | 4   | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN2                  | 5   | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN3                  | 6   | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN4                  | 11  | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN5                  | 12  | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN6                  | 13  | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| DRAIN7                  | 14  | O   | Open-drain output, LED current-sink channel, connect to LED cathode   |
| $\overline{\text{G}}$   | 8   | I   | Output enable, active-low. LED-channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off. |
| GND                     | 16  | —   | Power ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB.  |
| RCK                     | 10  | I   | Register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK.  |
| SER IN                  | 2   | I   | Serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.   |
| SER OUT                 | 9   | O   | Serial data output of the 8-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus.   |
| SRCK                    | 15  | I   | Serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.  |
| V <sub>CC</sub>         | 1   | I   | Power supply pin for the device. TI recommends adding a 0.1- $\mu\text{F}$ ceramic capacitor close to the pin.  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                      | MIN                                     | MAX | UNIT |
|------------------|--------------------------------------|---|-----|------|
| V <sub>CC</sub>  | Logic supply voltage                 | −0.3                                    | 8   | V    |
| V <sub>I</sub>   | Logic input-voltage range            | −0.3                                    | 8   | V    |
| V <sub>DS</sub>  | Power DMOS drain-to-source voltage   | −0.3                                    | 42  | V    |
|                  | Continuous total dissipation         | See <a href="#">Thermal Information</a> |     |      |
| T <sub>A</sub>   | Operating ambient temperature        | −40                                     | 125 | °C   |
| T <sub>J</sub>   | Operating junction temperature range | −40                                     | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range            | −55                                     | 165 | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         |   | VALUE                         | UNIT |      |
|--------------------|-------------------------|---|-------------------------------|------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000                         | V    |      |
|                    |                         | Charged device model (CDM), per AEC Q100-011            | All pins                      |      | ±750 |
|                    |                         |   | Corner pins (1, 8, 9, and 16) |      | ±750 |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

|                 |                               | MIN | MAX | UNIT |
|-----------------|-------------------------------|-----|-----|------|
| V <sub>CC</sub> | Supply voltage                | 3   | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage      | 2.4 |     | V    |
| V <sub>IL</sub> | Low-level input voltage       |     | 0.7 | V    |
| T <sub>A</sub>  | Operating ambient temperature | −40 | 125 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | TLC6C598-Q1                                  |          | UNIT |      |
|-------------------------------|--|----------|------|------|
|                               | PW (TSSOP)                                   | D (SOIC) |      |      |
|                               | 16 PINS                                      | 16 PINS  |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 129.4    | 100  | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 55.4     | 45   | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 65.8     | 40   | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 9.9      | 10   | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 65.2     | 40   | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | NA       | NA   | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                 |   | TEST CONDITIONS  |                       | MIN  | TYP   | MAX  | UNIT             |
|---|---|--|-----------------------|------|-------|------|------------------|
| DRAIN0 to DRAIN7. Drain-to-source voltage |   |  |                       |      |       | 40   | V                |
| $V_{OH}$                                  | High-level output voltage, SER OUT      | $I_{OH} = -20\ \mu\text{A}$  | $V_{CC} = 5\text{ V}$ | 4.9  | 4.99  |      | V                |
|   |   | $I_{OH} = -4\ \text{mA}$   |                       | 4.5  | 4.69  |      | V                |
| $V_{OL}$                                  | Low-level output voltage, SER OUT       | $I_{OH} = 20\ \mu\text{A}$   | $V_{CC} = 5\text{ V}$ |      | 0.001 | 0.01 | V                |
|   |   | $I_{OH} = 4\ \text{mA}$  |                       |      | 0.25  | 0.4  | V                |
| $I_{IH}$                                  | High-level input current                | $V_{CC} = 5\text{ V}$ , $V_I = V_{CC}$   |                       |      | 0.2   |      | $\mu\text{A}$    |
| $I_{IL}$                                  | Low-level input current                 | $V_{CC} = 5\text{ V}$ , $V_I = 0$  |                       |      | -0.2  |      | $\mu\text{A}$    |
| $I_{CC}$                                  | Logic supply current                    | $V_{CC} = 5\text{ V}$ , no clock signal  | All outputs off       |      | 0.1   | 1    | $\mu\text{A}$    |
|   |   |  | All outputs on        |      | 88    | 160  |                  |
| $I_{CC}(\text{FRQ})$                      | Logic supply current at frequency       | $f_{SRCK} = 5\text{ MHz}$ , $C_L = 30\text{ pF}$   | All outputs on        |      | 200   |      | $\mu\text{A}$    |
| $I_{DSX}$                                 | Off-state drain current                 | $V_{DS} = 30\text{ V}$   | $V_{CC} = 5\text{ V}$ |      |       | 0.1  | $\mu\text{A}$    |
|   |   | $V_{DS} = 30\text{ V}$ , $T_C = 125^\circ\text{C}$   | $V_{CC} = 5\text{ V}$ |      | 0.15  | 0.3  |                  |
| $r_{DS(\text{on})}$                       | Static drain-source on-state resistance | $I_D = 20\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , Single channel ON    |                       | 6    | 7.41  | 8.6  | $\Omega$         |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , All channels ON      |                       | 6.7  | 8.3   | 9.6  |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , Single channel ON  |                       | 7.9  | 9.34  | 11.2 |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , All channels ON    |                       | 8.7  | 10.25 | 12.3 |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 125^\circ\text{C}$ , Single channel ON   |                       | 9.1  | 11.13 | 12.9 |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 125^\circ\text{C}$ , All channels ON     |                       | 10.3 | 12.28 | 14.5 |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 125^\circ\text{C}$ , Single channel ON |                       | 11.6 | 13.69 | 16.4 |                  |
|   |   | $I_D = 20\text{ mA}$ , $V_{CC} = 3.3\text{ V}$ , $T_A = 125^\circ\text{C}$ , All channels ON   |                       | 12.8 | 14.89 | 18.2 |                  |
| $T_{\text{SHUTDOWN}}$                     | Thermal shutdown trip point             |  |                       | 150  | 175   | 200  | $^\circ\text{C}$ |
| $T_{\text{hys}}$                          | Hysteresis                              |  |                       |      | 15    |      | $^\circ\text{C}$ |

## 6.6 Timing Requirements

|          |  | MIN | NOM | MAX | UNIT |
|----------|--|-----|-----|-----|------|
| $t_{su}$ | Setup time, SER IN high before SRCK $\uparrow$ | 15  |     |     | ns   |
| $t_h$    | Hold time, SER IN high after SRCK $\uparrow$   | 15  |     |     | ns   |
| $t_w$    | SER IN pulse duration                          | 40  |     |     | ns   |

**TLC6C598-Q1**

SLIS142D – DECEMBER 2012 – REVISED SEPTEMBER 2016

[www.ti.com](http://www.ti.com)
**6.7 Switching Characteristics**
 $V_{CC} = 5\text{ V}$ ,  $T_J = 25^\circ\text{C}$ 

| PARAMETER      |  | TEST CONDITIONS                             | MIN | TYP  | MAX | UNIT |
|----------------|--|---|-----|------|-----|------|
| $t_{PLH}$      | Propagation delay time, low-to-high-level output from $\overline{G}$ | $C_L = 30\text{ pF}$ , $I_D = 48\text{ mA}$ |     | 220  |     | ns   |
| $t_{PHL}$      | Propagation delay time, high-to-low-level output from $\overline{G}$ |   |     | 75   |     | ns   |
| $t_r$          | Rise time, drain output  |   |     | 210  |     | ns   |
| $t_f$          | Fall time, drain output  |   |     | 128  |     | ns   |
| $t_{pd}$       | Propagation delay time, SRCK $\downarrow$ to SER OUT                 | $C_L = 30\text{ pF}$ , $I_D = 48\text{ mA}$ |     | 49.4 |     | ns   |
| $t_{or}$       | SER OUT rise time (10% to 90%)                                       | $C_L = 30\text{ pF}$                        |     | 20   |     | ns   |
| $t_{of}$       | SER OUT fall time (90% to 10%)                                       | $C_L = 30\text{ pF}$                        |     | 20   |     | ns   |
| $f_{(SRCK)}$   | Serial clock frequency   | $C_L = 30\text{ pF}$ , $I_D = 20\text{ mA}$ |     |      | 10  | MHz  |
| $t_{SRCK\_WH}$ | SRCK pulse duration, high  |   | 30  |      |     | ns   |
| $t_{SRCK\_WL}$ | SRCK pulse duration, low   |   | 30  |      |     | ns   |

### 6.8 Timing Waveforms

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 13). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

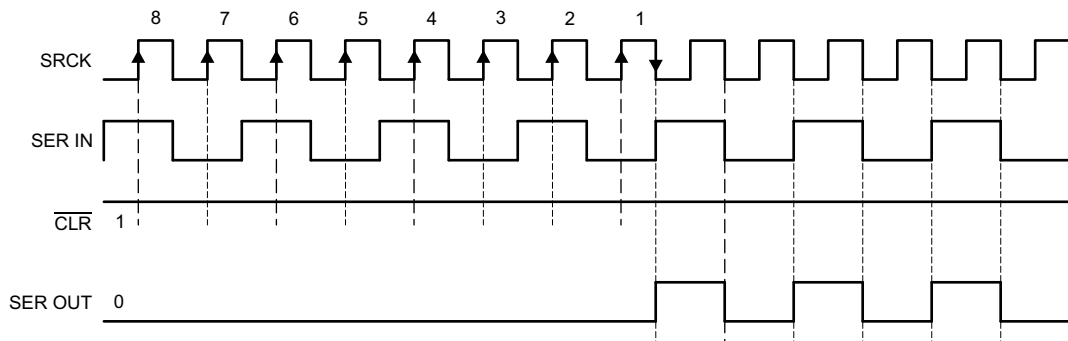


Figure 1. SER IN to SER OUT Waveform

Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 11.

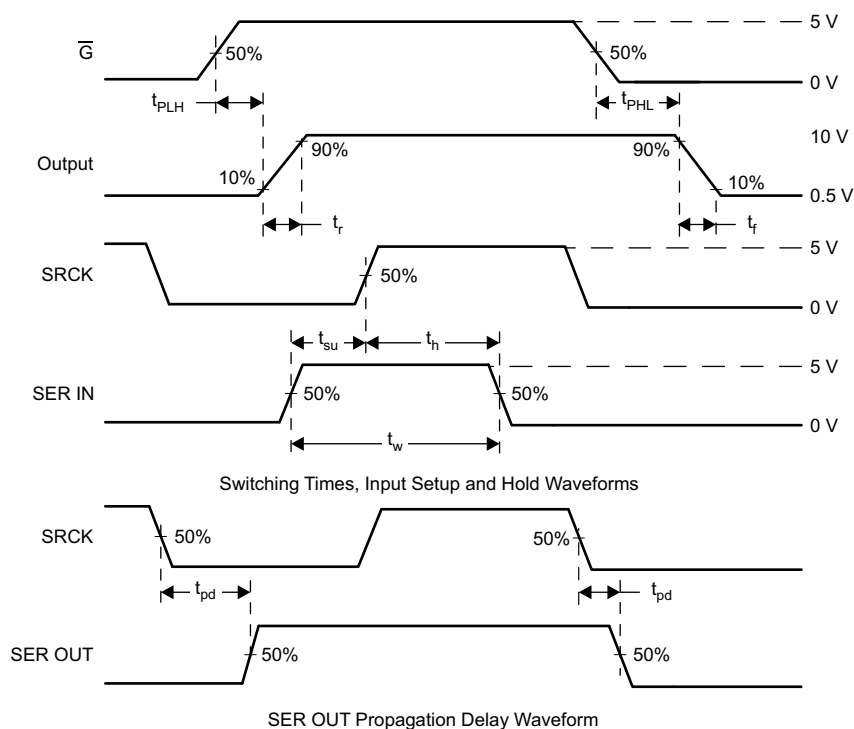


Figure 2. Switching Times and Voltage Waveforms

### 6.9 Typical Characteristics

Conditions for Figure 5 and Figure 6: Single channel on, conditions for Figure 7, Figure 8 and Figure 9: All channels on

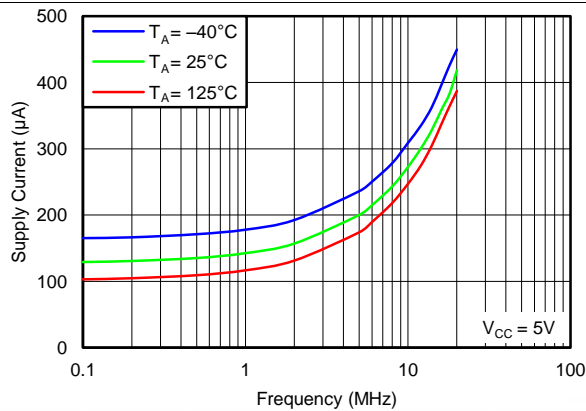


Figure 3. Supply Current vs Frequency

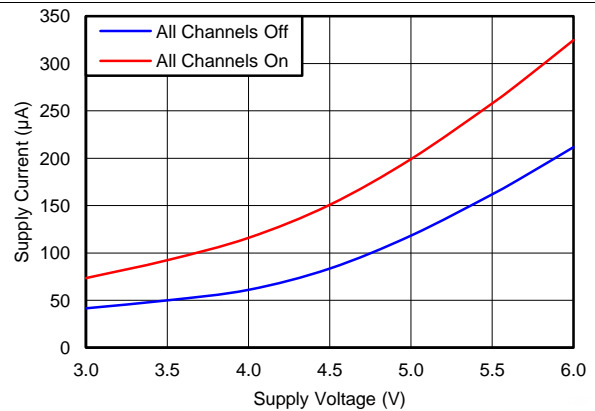


Figure 4. Supply Current vs Supply Voltage

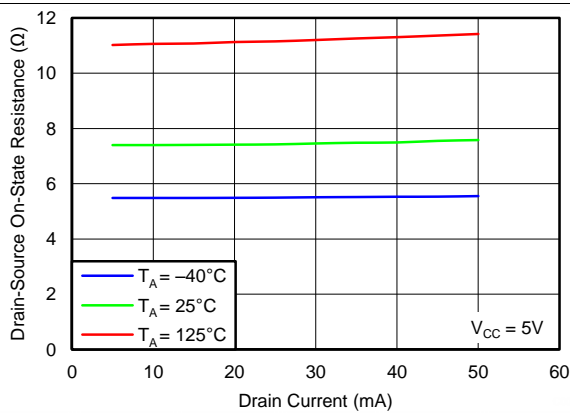


Figure 5. Drain-to-Source On-State Resistance vs Drain Current

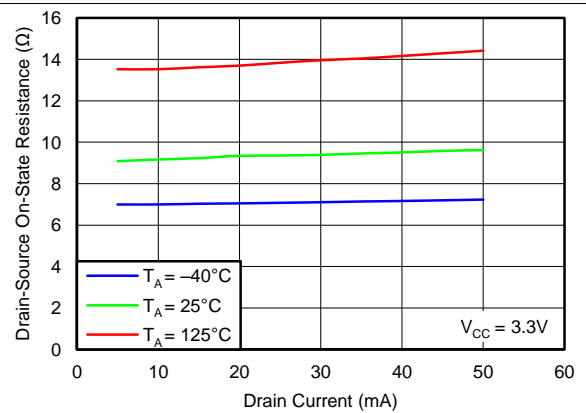


Figure 6. Drain-to-Source On-State Resistance vs Drain Current

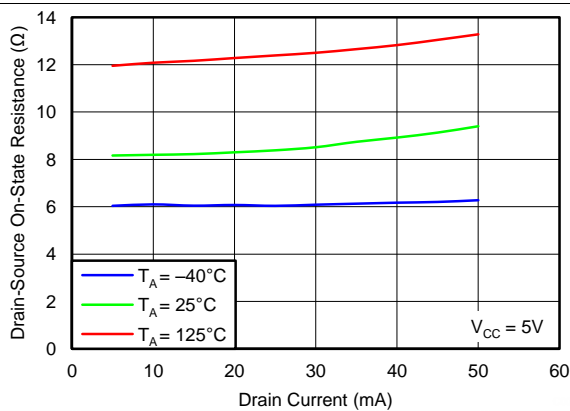


Figure 7. Drain-to-Source On-State Resistance vs Drain Current

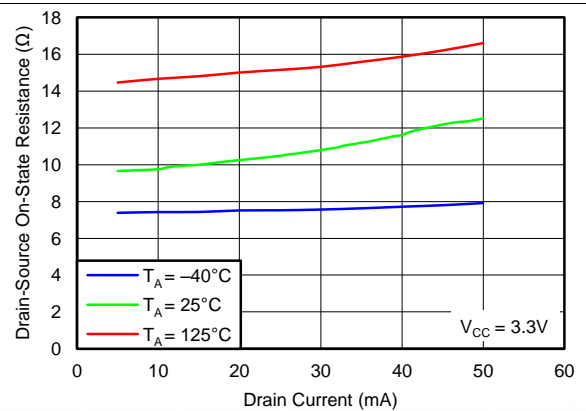
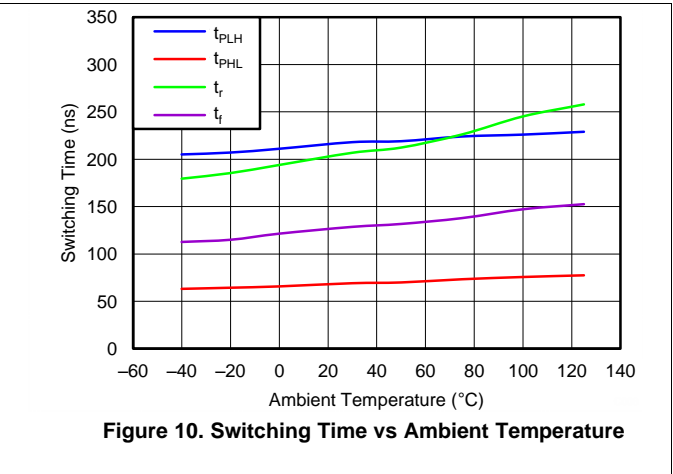
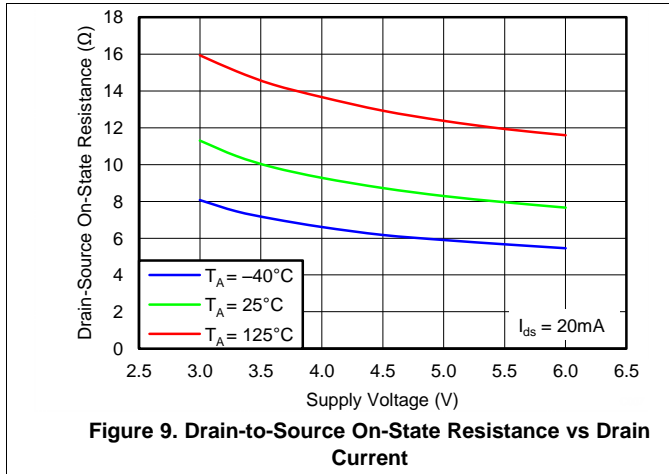


Figure 8. Drain-to-Source On-State Resistance vs Drain Current



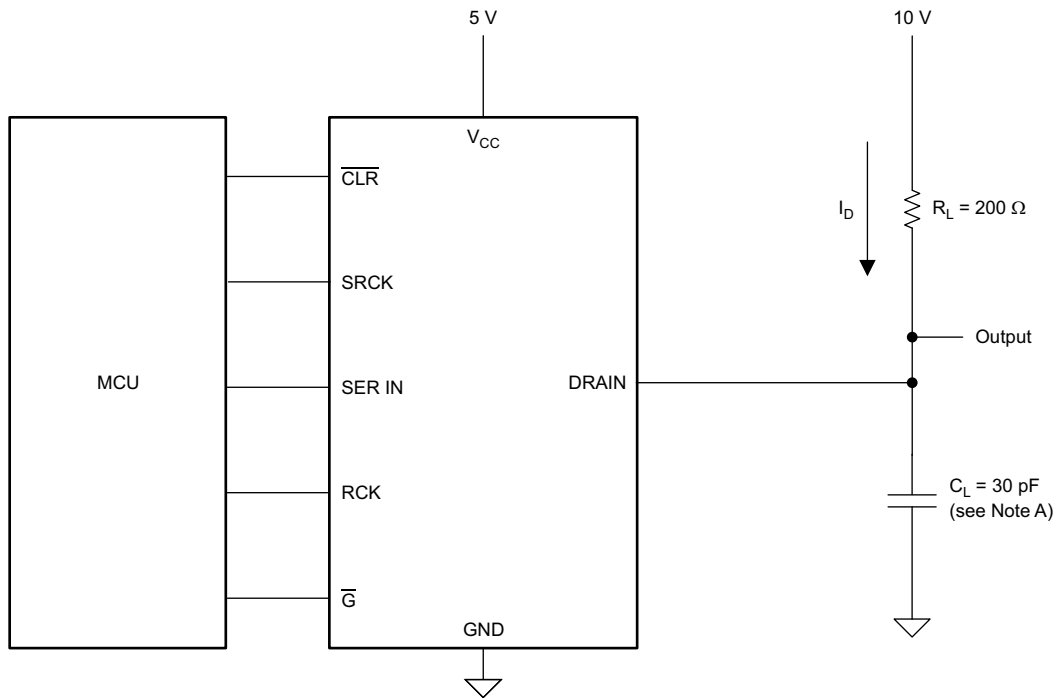
Typical Characteristics (continued)

Conditions for Figure 5 and Figure 6: Single channel on, conditions for Figure 7, Figure 8 and Figure 9: All channels on



7 Parameter Measurement Information

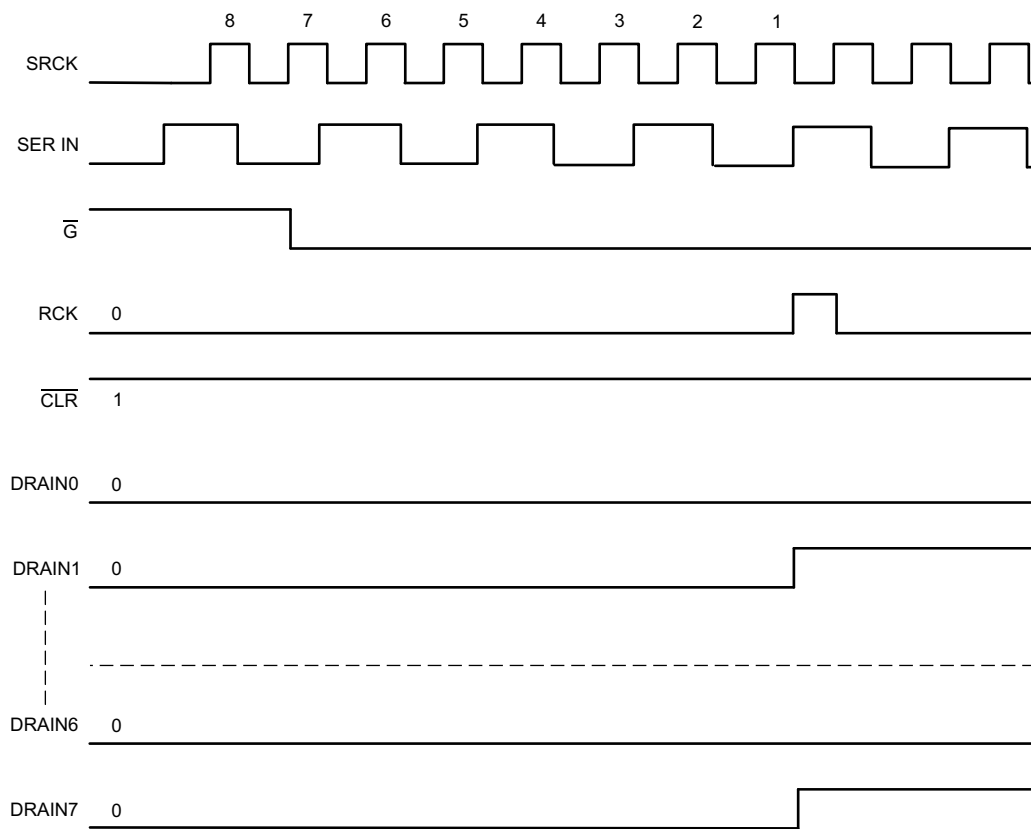
Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with G held low and CLR held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.



Copyright © 2016, Texas Instruments Incorporated

A. C<sub>L</sub> includes probe and jig capacitance.

Figure 11. Resistive-Load Test Circuit

**Parameter Measurement Information (continued)**

**Figure 12. Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TLC6C598-Q1 device is a monolithic, medium-voltage, low-current 8-bit shift register designed to drive relatively moderate load power such LEDs. The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Thermal shutdown protection is also built-into the device.

### 8.2 Functional Block Diagram

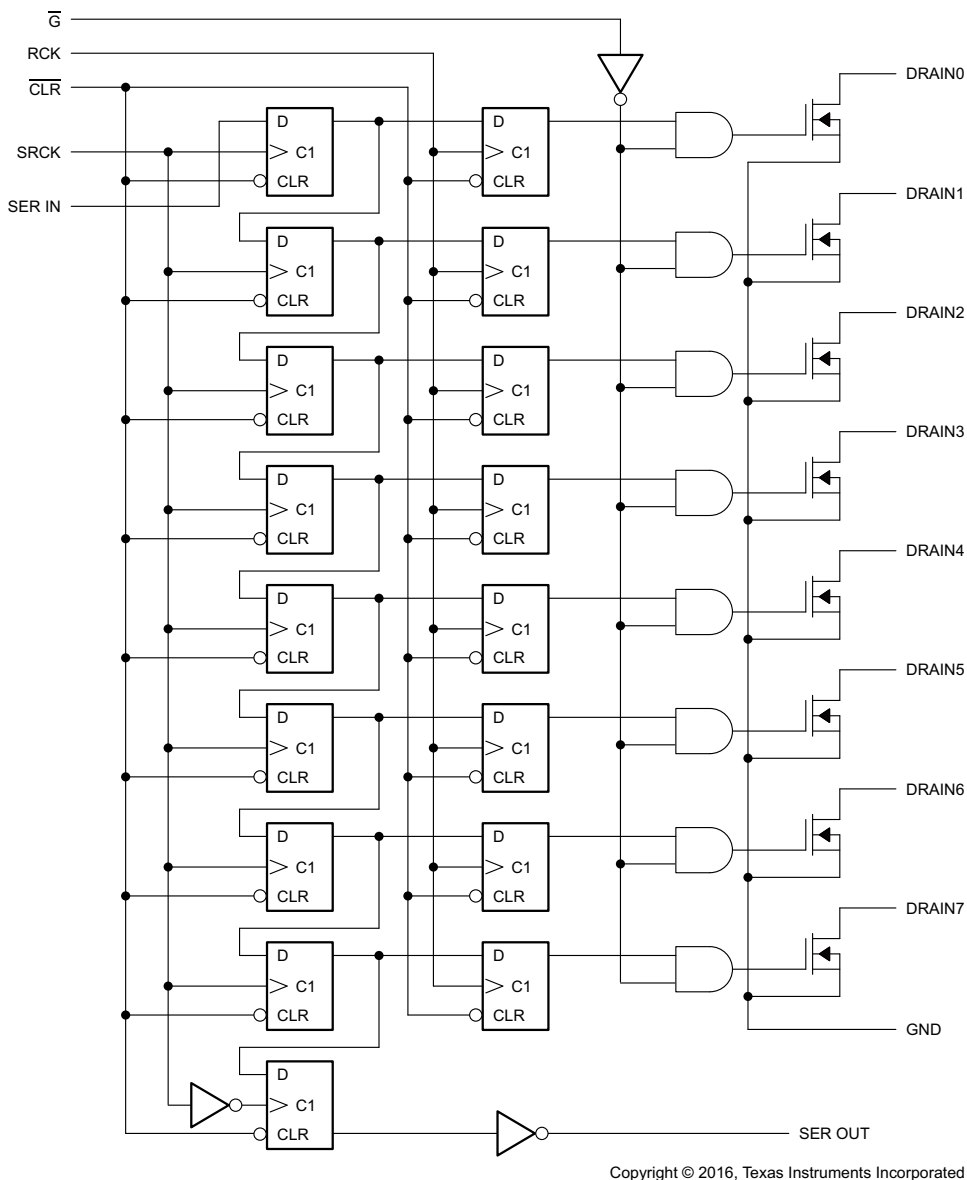


Figure 13. Logic Diagram (Positive) of TLC6C598-Q1

## 8.3 Feature Description

### 8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

### 8.3.2 Serial-In Interface

The TLC6C598-Q1 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfer through the shift and storage registers is on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high.

### 8.3.3 Clear Registers

A logic low the CLR pin clears all registers in the device. TI suggests clearing the device during power up or initialization.

### 8.3.4 Output Channels

DRAIN0–DRAIN7. These pins can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.

### 8.3.5 Register Clock

RCK is the storage-register clock. Data in the storage register appears at the output whenever the output enable ( $\bar{G}$ ) input signal is high.

### 8.3.6 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.

### 8.3.7 Output Control

Holding the output enable (pin G) high holds all data in the output buffers low, and all drain outputs are off. Holding G low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sinking current. This pin also can be used for global PWM dimming.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $V_{CC} < 3\text{ V}$

This device works normally within the range  $3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ . When the operating voltage is lower than 3 V, correct behavior of the device, including communication interface and current capability, is not assured.

### 8.4.2 Operation With $5.5\text{ V} \leq V_{CC} \leq 8\text{ V}$

The device works normally in this voltage range, but reliability issues may occur if the device works for a long time in this voltage range.

## 9 Application and Implementation

---

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

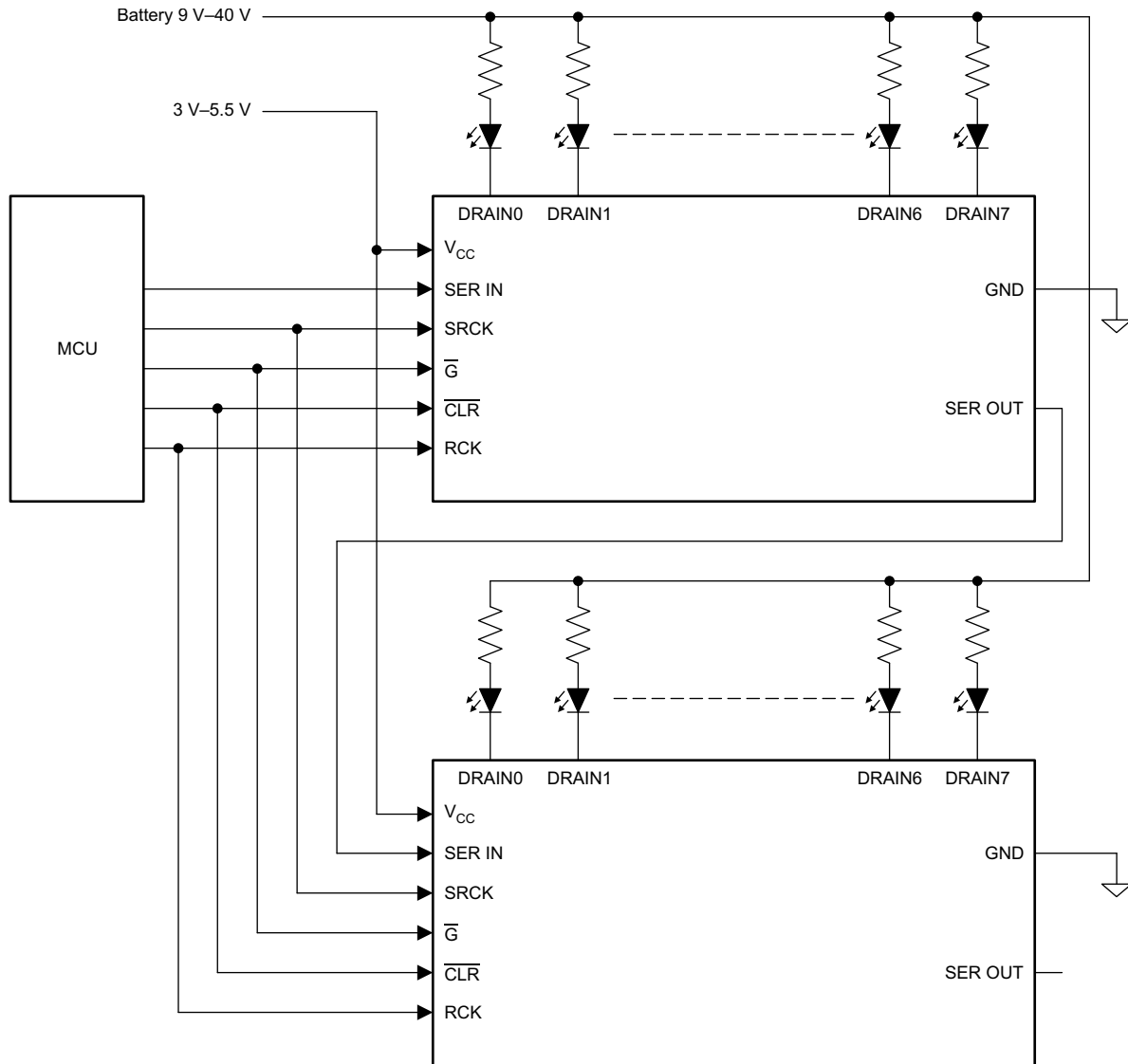
### 9.1 Application Information

The TLC6C598-Q1 device is a serial-in, parallel-out, power and logic, 8-bit shift register with low-side open-drain DMOS output ratings of 40-V and 50-mA continuous sink-current capabilities when  $V_{CC} = 5\text{ V}$ . The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model

### 9.2 Typical Application

[Figure 14](#) shows a typical cascade application circuit with two TLC6C598-Q1 chips configured in cascade topology. The MCU generates all the input signals.

Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 14. Typical Application Circuit

9.2.1 Design Requirements

| DESIGN PARAMETER   | EXAMPLE VALUE |
|--|---------------|
| V <sub>Battery</sub>   | 9 V to 40 V   |
| V <sub>CC_1</sub>  | 3.3 V         |
| I(D0), I(D1), I(D2), I(D3), I(D4), I(D5), I(D6), I(D7)       | 30 mA         |
| V <sub>CC_2</sub>  | 5 V           |
| I(D8), I(D9), I(D10), I(D11), I(D12), I(D13), I(D14), I(D15) | 50 mA         |

### 9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- $V_{\text{supply}}$ : LED supply voltage
- $V_{\text{Dx}}$ : LED forward voltage
- $I$ : LED current

With these parameters determined, the resistor in series with the LED can be calculated by using the following equation:

$$R_X = (V_{\text{Supply}} - V_{\text{Dx}}) / I \quad (1)$$

### 9.2.3 Application Curve

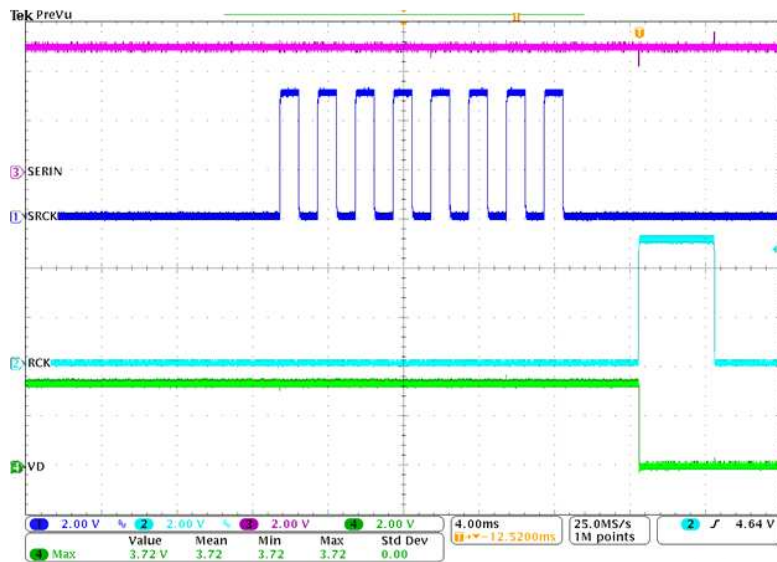


Figure 15. TLC6C598-Q1 Application Waveform

## 10 Power Supply Recommendations

The TLC6C598-Q1 device is designed to operate with an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the  $V_{CC}$  pin.

## 11 Layout

### 11.1 Layout Guidelines

There are no special layout requirement for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pin.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the cooper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.

All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

### 11.2 Layout Example

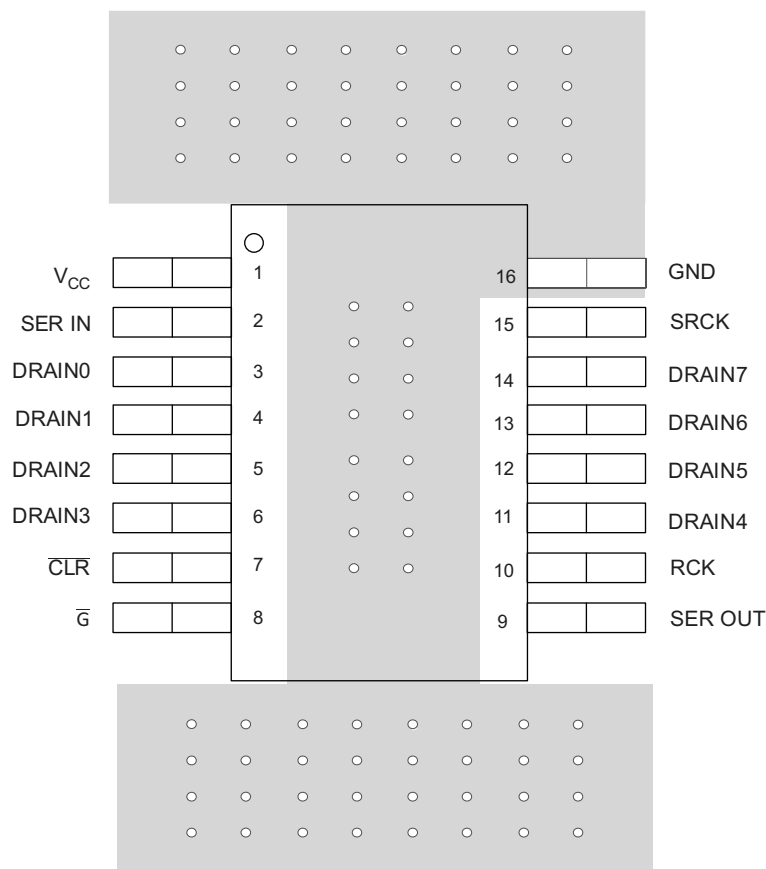


Figure 16. TLC6C598-Q1 Example Layout



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**TLC6C598-Q1**

SLIS142D – DECEMBER 2012 – REVISED SEPTEMBER 2016

[www.ti.com](http://www.ti.com)
**13.1 Package Option Addendum**
**13.1.1 Packaging Information**

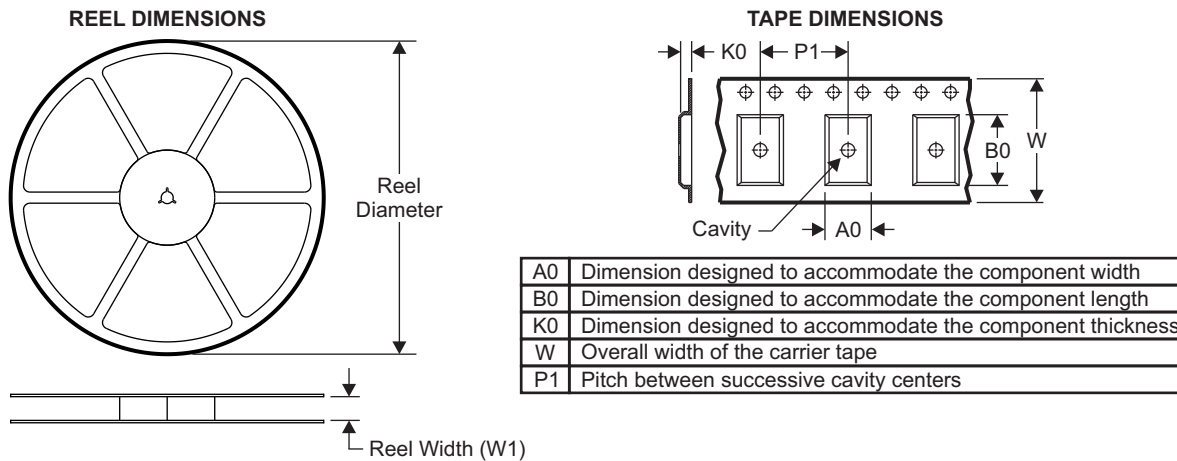
| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish <sup>(3)</sup> | MSL Peak Temp <sup>(4)</sup> | Op Temp (°C) | Device Marking <sup>(5)(6)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|----------------------------------|
| TLC6C598QPWRQ1   | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU                       | Level-3-260C-168 HR          | -40 to 125   | 6C598                            |
| TLC6C598QDRQ1    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU                       | Level-3-260C-168 HR          | -40 to 125   | TLC6C598                         |
| TLC6C598CQDRQ1   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU                       | Level-3-260C-168 HR          | -40 to 125   | TLC6C598C                        |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

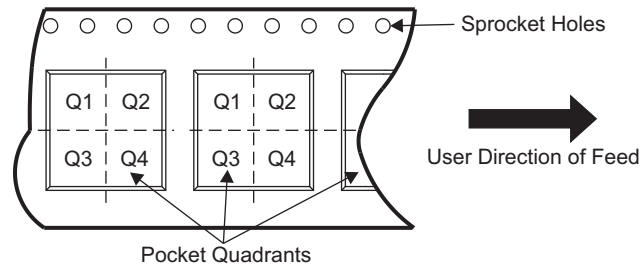
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**13.1.2 Tape and Reel Information**



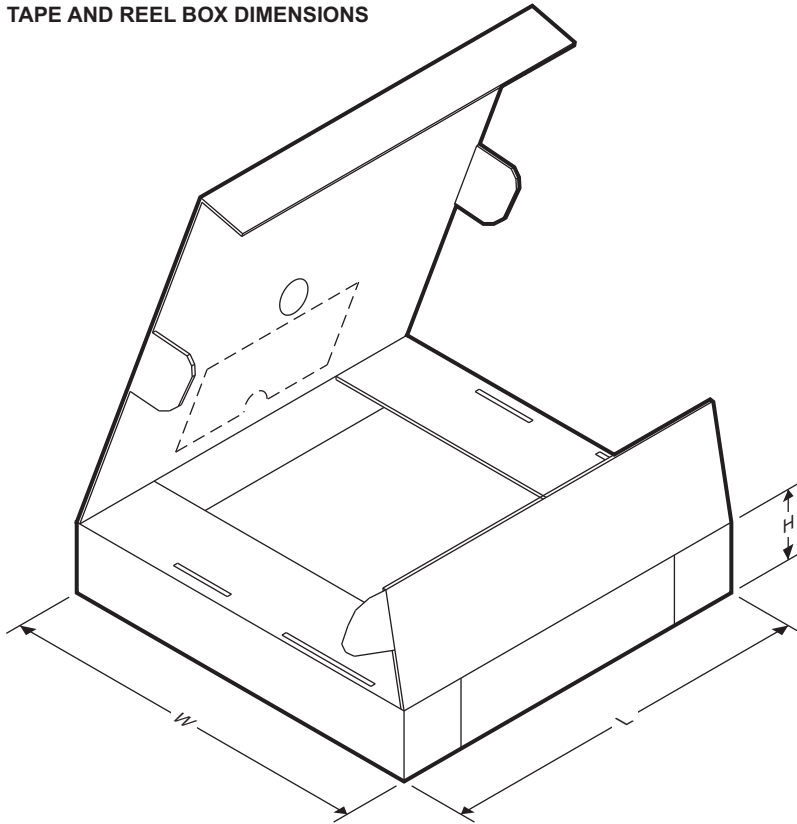
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC6C598QPWRQ1 | TSSOP        | PW              | 16   | 2000 | 330                | 12.4               | 6.9     | 5.6     | 1.6     | 8       | 12     | Q1            |
| TLC6C598QDRQ1  | SOIC         | D               | 16   | 2500 | 330                | 16.4               | 6.5     | 10.3    | 2.1     | 8       | 16     | Q1            |
| TLC6C598CQDRQ1 | SOIC         | D               | 16   | 2500 | 330                | 16.4               | 6.5     | 10.3    | 2.1     | 8       | 16     | Q1            |

**TLC6C598-Q1**

SLIS142D – DECEMBER 2012 – REVISED SEPTEMBER 2016



[www.ti.com](http://www.ti.com)
**TAPE AND REEL BOX DIMENSIONS**


| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC6C598QPWRQ1 | TSSOP        | PW              | 16   | 2000 | 367         | 367        | 38          |
| TLC6C598QDRQ1  | SOIC         | D               | 16   | 2500 | 367         | 367        | 38          |
| TLC6C598CQDRQ1 | SOIC         | D               | 16   | 2500 | 367         | 367        | 38          |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

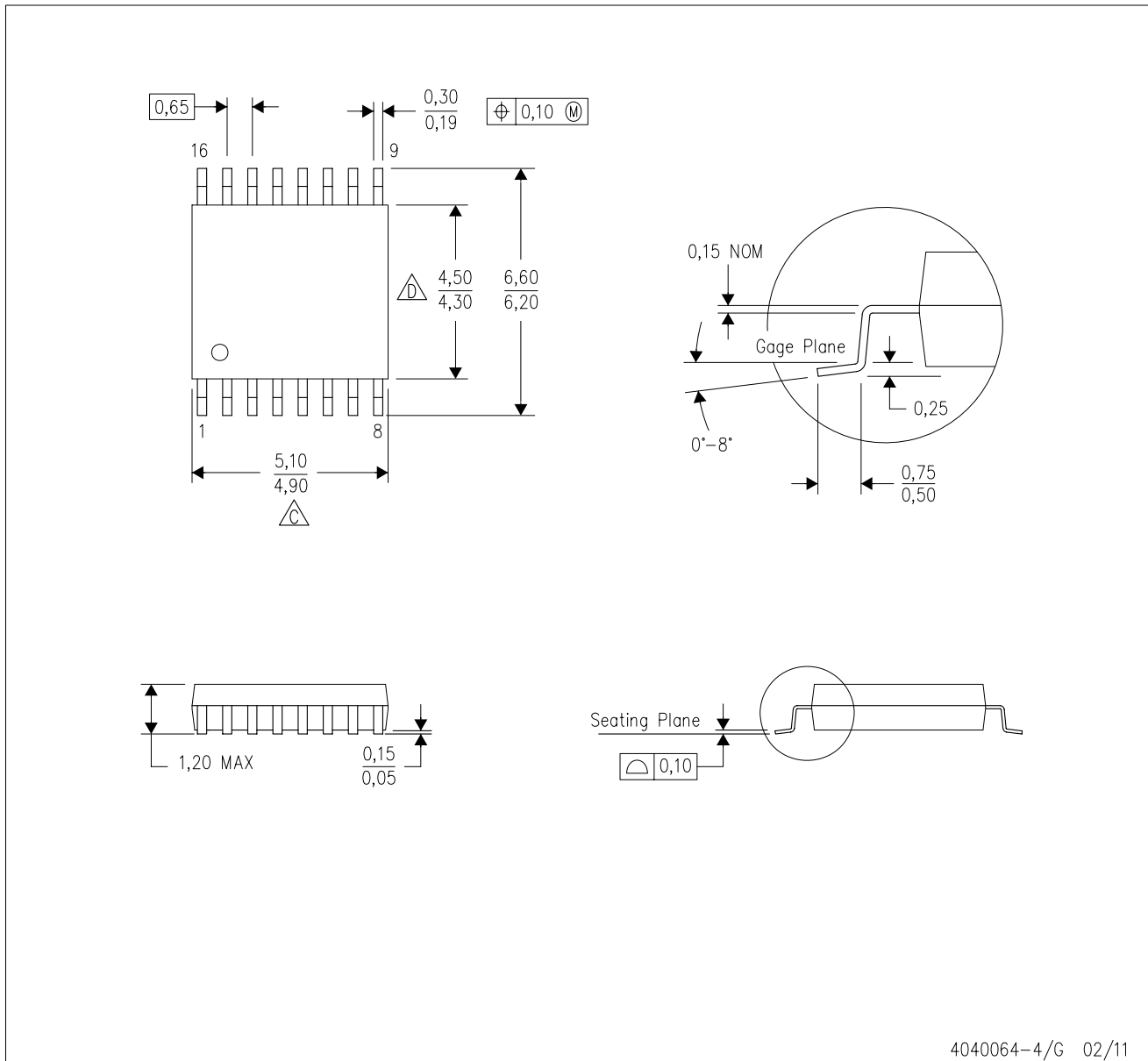
PLASTIC SMALL OUTLINE





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.