

# SPECIFICATIONS

Customer	伟创捷
Product Name	<b>Solid Tantalum Chip Capacitors</b>
Sunlord Part Number	TC212A226M010A
Customer Part Number	

New Released,  Revised]

SPEC No.: **TC08170028**

【This SPEC is total 10 pages including specifications and appendix.】

【ROHS Compliant Parts】

Approved By	Checked By	Issued By
		

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### 【For Customer approval Only】

Date: \_\_\_\_\_

Qualification Status: Full  Restricted  Rejected

Approved By	Verified By	Re-checked By	Checked By

Comments:

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**【Version change history】**

Rev.	Effective Date	Changed Contents	Change reasons	Approved By
01	Sep.13, 2017	New release	/	Hai Guo

1. Scope

This specification applies to TC212A226M010A of Solid Tantalum Chip Capacitors.

2. Reference

- EIA Standard 535BAAC-A Fixed Tantalum Chip Capacitor Style 1 Protected (molded)
- GJB 2283-95 Established reliability general specification for fixed solid electrolytic tantalum chip capacitor
- GJB 360A-96 Test methods for electronic and electrical component parts
- IEC384-3-1 Test Methods for Environmental Testing

3. Product Description and Identification (Part Number)

a) Description

TC212A226M010A of Solid Tantalum Chip Capacitors.

b) Product Identification (Part Number)

TC     212     A     226     M     010     A  
 ①        ②        ③        ④        ⑤        ⑥        ⑦

①	Type
TC	Chip Tantalum Capacitor

②	Series
212	Low ESR

③	External Dimensions (L×W) (mm)
A	3.2×1.6

④	Nominal Capacitance
Example	Nominal Value
226	22×10 <sup>6</sup> pF

⑤	Capacitance Tolerance
M	±20%

⑥	Rated DC Voltage
Example	Rated DC Voltage
010	10V

⑦	Internal Code
A	Black Molded Case

3) Markings

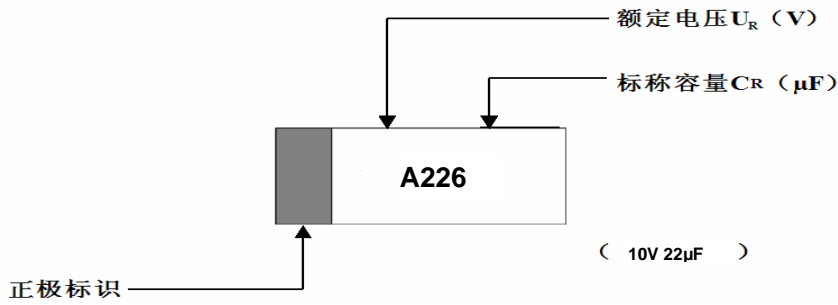
Rated Voltage Code

Rated Voltage (V)	10
Code	A

Capacitance Code

Capacitance (μF)	22
Code (B Case)	226

Markings:



4. Electrical Characteristics

Capacitance ( $\mu F$ )	Case	Sunlord P/N	Leakage Current ( $\mu A$ ) 25°C Max.	DF (%) +25°C 120Hz Max.	ESR( $\Omega$ )+25°C 100kHz Max.
10V, +85°C (6.3V @ +125°C)					
22.0	A	TC212A226M010A	2.2	8.0	2.5

- 1) Operating and storage temperature range (individual chip without packing): -55°C~+125°C
- 2) Storage temperature range (packaging conditions): -10°C~+40°C, RH70% (MAX).

5. Shape and Dimensions

- a) Dimensions and recommended PCB pattern for reflow soldering: See Fig.5-1, Fig.5-2 and Table 5-1
- b) Structure: See Fig. 5-3

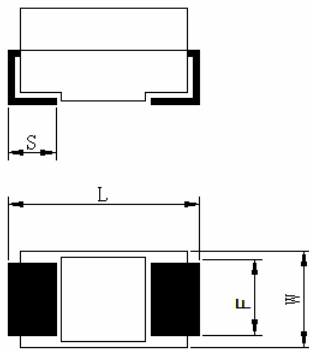


Fig.5-1

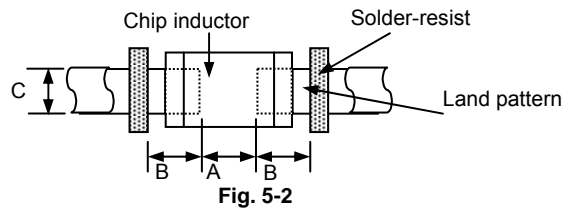


Fig. 5-2

Tab.5-1

Unit: mm [inch]

Case Code	Type	L	W	H	F( $\pm 0.10$ ) [ $\pm 0.04$ ]	S( $\pm 0.30$ ) [ $\pm 0.12$ ]	A	B	C
A	3216-18	3.2 $\pm 0.20$ [.126 $\pm 0.008$ ]	1.6 $\pm 0.20$ [.063 $\pm 0.008$ ]	1.6 $\pm 0.20$ [.063 $\pm 0.008$ ]	1.2 [.047]	0.8 [.031]	1.1	1.35	1.5

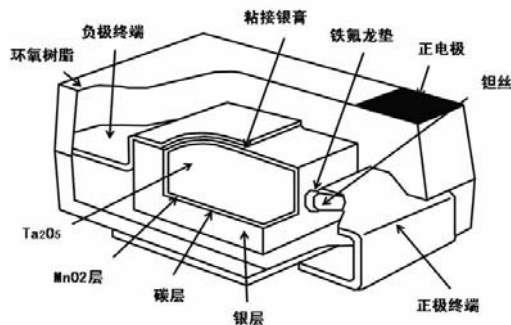


Fig.5-3

## 6. Test and Measurement Procedures

### 6.1 Test Conditions

Unless other specified, the standard atmospheric conditions for measurement/test as:

- ① Ambient Temperature:  $25 \pm 10^\circ\text{C}$
- ② Relative Humidity:  $50 \pm 30\%$
- ③ Air Pressure:  $86\text{kPa} \sim 106\text{kPa}$

If any doubt on the results, measurements/tests should be made within the following limits:

- a. Ambient Temperature:  $25 \pm 1^\circ\text{C}$
- b. Relative Humidity:  $50 \pm 2\%$
- c. Air Pressure:  $86\text{kPa} \sim 106\text{kPa}$

### 6.2 Visual Examination

Inspection Equipment: visual;

### 6.3 Electrical Test

#### 6.3.1 Equivalent Series Resistance (ESR)

- ① Test frequency:  $100 \pm 5\text{kHz}$ , Refer to **Electrical Characteristics**
- ② Test equipment (Analyzer): HP4263B or equal ESR Tester

#### 6.3.2 Capacitance (C)

- ① Test frequency :  $120 \pm 5\text{Hz}$ , Refer to **Electrical Characteristics**
- ② Test equipment: HP4263B or equal capacitance tester
- ③ Test signal:  $1000\text{mV}$

#### 6.3.3 Dissipation Factor ( $\tan \delta$ )

- a. Test frequency:  $120 \pm 5\text{Hz}$ , Refer to **Electrical Characteristics**
- b. Test equipment: HP4263B or equal capacitance tester
- c. Test signal:  $1000\text{mV}$

#### 6.3.4 Leakage Current ( $I_0$ )

- a. Refer to **Electrical Characteristics**
- b. Test equipment: TH2686 or equivalent  $I_0$  test equipment.
- c. Measurement method:
  - 1) The chip shall be charged for 5min at most at rated voltage at  $25^\circ\text{C}$
  - 2) Current decreases as time passes, but gets into a stable situation at a certain value which shall be recorded as  $I_0$ .

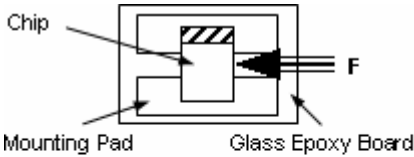
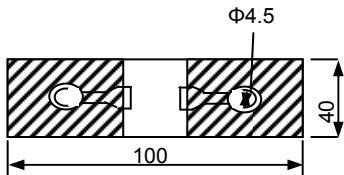
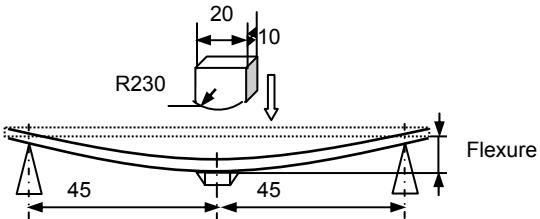
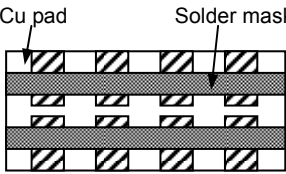
#### 6.3.5 Rated Voltage ( $U_R$ )

Rated voltage is the maximum DC operating voltage for continuous duty at  $-55^\circ\text{C} \sim 85^\circ\text{C}$ . Capacitor may be operated at  $125^\circ\text{C}$  with voltage derating to two-thirds of rated voltage. The derated voltages at different operating temperatures are listed in the table below.

Surge voltage is the maximum voltage to which capacitors may be subjected under any momentary conditions, including the maximum AC pulse voltage, DC bias voltage and any momentary voltage. Refer to the table below for detail data.

Rated Voltage ( $U_R$ )	2.5V	4V	6.3V	10V	16V	20V	25V	35V	50V	@ $-55^\circ\text{C} \sim 85^\circ\text{C}$
Derated voltage ( $U_C$ )	1.6V	2.5V	4V	6.3V	10V	13V	16V	20V	32V	@ $125^\circ\text{C}$
Surge Voltage ( $U_S$ )	3.3V	5.2V	8V	13V	20V	26V	32V	46V	65V	@ $-55^\circ\text{C} \sim 85^\circ\text{C}$
Surge Voltage ( $U_S$ )	2.2V	3.4V	5V	8V	13V	16V	20V	28V	40V	@ $125^\circ\text{C}$

6.4 Reliability Test

Item	Requirements	Test Methods and Remarks
<p>6.4.1 Terminal Strength</p>	<p>No removal or split of the termination or other defects shall occur.</p>  <p>Fig.6.4.1-1</p>	<p>a. Solder the capacitor inductor to the testing jig (glass epoxy board shown in Fig. 6.4.1-1) using eutectic solder. Then apply a force in the direction of the arrow.</p> <p>b. 5N force</p> <p>c. Keep time: 10±1s</p> <p>d. Speed: 1.0mm/s</p>
<p>6.4.2 Resistance to Flexure</p>	<p>No visible mechanical damage.</p> <p>Unit: mm</p>  <p>Fig.6.4.2-1</p>	<p>① Solder the capacitor to the test jig (glass epoxy board shown in Tab. 5-1) Using a eutectic solder. Then apply a force in the direction shown in Fig. 6.4.2-1~Fig. 6.4.2-2</p> <p>② Flexure:1 mm;</p> <p>③ Pressurizing Speed: 0.5mm/sec.</p> <p>④ Keep time: 10 sec.</p>  <p>Fig.6.4.2-2</p>
<p>6.4.3 Vibration</p>	<p>No visible mechanical damage.</p>  <p>Fig.6.4.3-1</p>	<p>① Solder the capacitor to the testing jig (glass epoxy board shown in Fig.6.4.3-1) using eutectic solder.</p> <p>② The capacitor shall be subjected to a simple harmonic motion having total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz.</p> <p>③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3 mutually perpendicular directions (total of 6 hours).</p>

<p>6.4.4 Solderability</p>	<p>① No visible mechanical damage. ② Wetting shall exceed 95% coverage.</p>	<p>① Solder temperature: 240±2°C ② Duration: 3 sec. ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight.</p>
<p>6.4.5 Resistance to Soldering Heat</p>	<p>a. No visible mechanical damage. b. Wetting shall exceed 95% coverage. c. Capacitance change: within ±5%. d. tanδ shall not exceed 150% of the initial requirement. e. LC shall not exceed the initial I<sub>0</sub>.</p>	<p>① Reflow soldering: please refer to <b>Fig. 8-1</b>. ② The chip shall be stabilized at normal condition for 1~2 hours before measuring.</p>
<p>6.4.6 Temperature</p>	<p>① At -55°C ① No visible mechanical damage. ② Capacitance change: within - 10%. ③ tanδ shall not exceed 150% of the initial requirement.</p> <p>② At 85°C ① No visible mechanical damage. ② Capacitance change: within 10% ③ tanδ shall not exceed 150% of the initial requirement. ④ L C shall not exceed 10 I<sub>0</sub></p> <p>③ At 125°C ① No visible mechanical damage. ② Capacitance change: within 12%. ③ tanδ shall not exceed 150% of the initial requirement. ④ LC shall not exceed 12.5 I<sub>0</sub>.</p>	<p>① Drying 30<sup>+4</sup> min at 125°C ② The chip shall be stabilized at normal condition for 1~2 hours after drying, and measured at 25°C as initial data. ③ The chip shall be measured at -55°C</p> <p>① After Step A, the chip shall cool to room temperature. ② Measure at 85°C.</p> <p>① After Step B, the chip shall be measured at 125°C.</p>
<p>6.4.7 Thermal Shock</p>	<p>① Capacitance change: within ±5%. ② tanδ shall not exceed the initial requirement. ③ LC shall not exceed the initial I<sub>0</sub>.</p>	<p>① Temperature, Time (<b>Fig.6.4.7</b>) ② -55°C, 30±3 min→125°C, 30±3min. ③ Transforming interval: Max.5min. ④ Tested cycle: 5 cycles. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.</p> <div data-bbox="911 1189 1342 1417" style="text-align: center;"> <p>The diagram shows a thermal shock test profile. It starts at Room Temperature (RT), drops to -55°C, and dwells for 30 minutes. It then rises to 125°C and dwells for 30 minutes. The transition between -55°C and 125°C is labeled as 5min(max). The cycle repeats.</p> </div> <p><b>Fig.6.4.7</b></p>
<p>6.4.8 Moisture Resistance</p>	<p>① No visible mechanical damage. ② Capacitance change: ±10%. ③ tanδ shall not exceed 150% of the initial requirement. ④ L C shall not exceed 2I<sub>0</sub>.</p>	<p>① Temperature: 40±2°C. ② Relative Humidity: 90%~95%RH. ③ Duration: 500<sup>+24</sup> hours. ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring.</p>
<p>6.4.9 Life Test</p>	<p>6. No visible mechanical damage. 7. Capacitance change: ±10%. 8. tanδ shall not exceed the initial requirement. 9. L C shall not exceed 1.25 I<sub>0</sub>.</p>	<p>① Temperature: 85±2°C; Rated Voltage ② Duration: 2000<sup>+24</sup> hours ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.</p>

7. Packaging, Storage and Transportation

7.1 Packaging

7.1.1 Tape Carrier Packaging:

Refer to Fig.7.1-1~3 for detail. Tape carrier packaging quantity is listed in the following table:

Case code	EIA size	Package quantity
A	3216	2000

(1) Taping Drawings (Unit: mm)

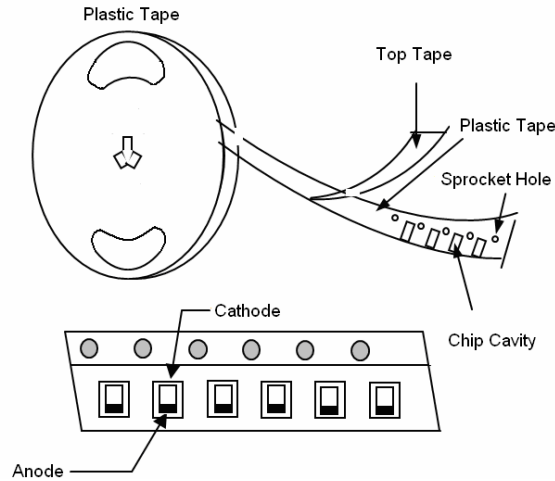


Fig.7.1-1

Remark: The sprocket holes are to the right as the tape is pulled toward the user.

(2) Taping Dimensions (Unit: mm)

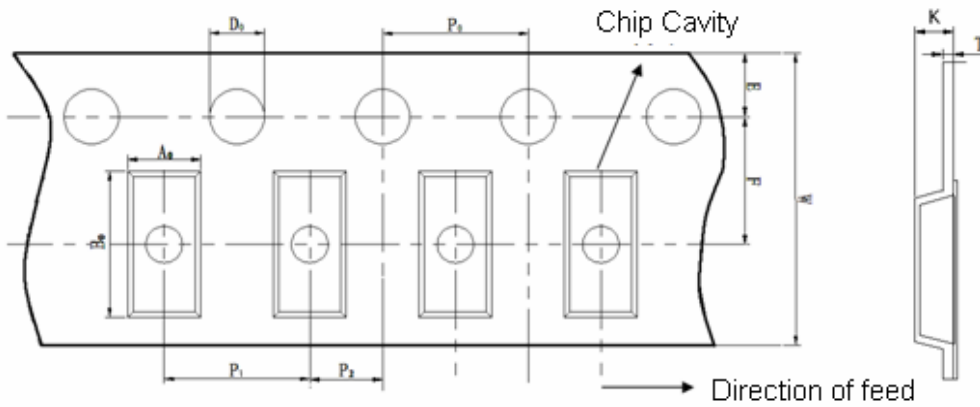


Fig.7.1-2

Case	W	$A_0$	$B_0$	$P_0$	F	K max	T max
A	$8.0 \pm 0.3$	$1.90 \pm 0.20$	$3.50 \pm 0.20$	$4.0 \pm 0.1$	$3.5 \pm 0.05$	2.1	0.3



(3) Reel Dimensions (Unit: mm)

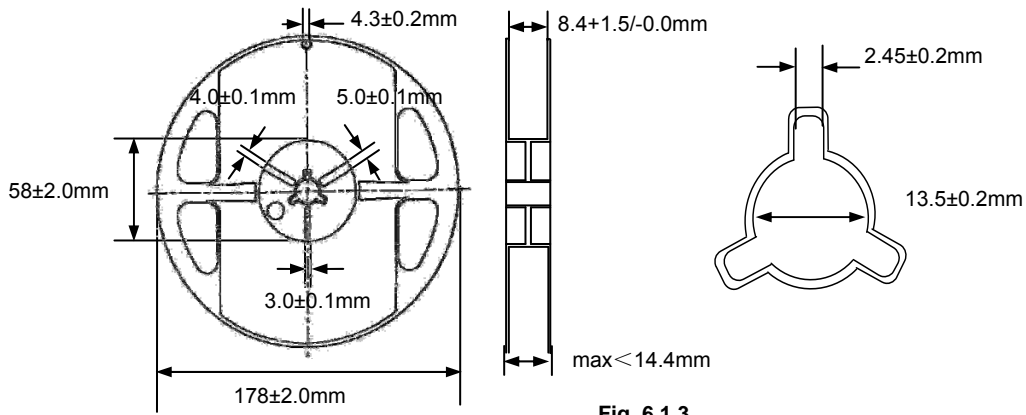


Fig. 6.1.3

Case code	Tape width	W
A	8mm	10mm

7.2 Storage

- a) The solderability of the external electrode may be deteriorated if packages are stored where they are exposed to high humidity. Package must be stored at 40°C or less and 70% RH or less.
- b) The solderability of the external electrode may be deteriorated if packages are stored where they are exposed to dust or harmful gas (e.g. HCl, sulfurous gas of H<sub>2</sub>S).
- c) Packaging material may be deformed if package are stored where they are exposed to heat of direct sunlight.
- d) The minimum package and polyethylene package should not be opened until the capacitors are used; once they were opened, use the capacitors as soon as possible.
- e) Solderability specified shall be guaranteed for 3 months from the date of delivery on condition that they are stored at the environment specified in **Clause 4**. For those parts, which passed more than 3 months shall be checked solder-ability before use.

7.3 Transportation

Package should not be destroyed or get wet.

7.4 Precautionary measures

- a) Put on electrostatic prevention to avoid ESD.
- b) Equipments involved in capacitor application (such as soldering tip and tester) should be well grounded.
- c) Avoid touching electrode directly by hand or metal (such as metal table).

7.5 Cautions for Using Tantalum Capacitor

7.5.1 Operating voltage

The ratio of operating voltage to rated voltage has a great influence on capacitor failures. Please take all specified reliabilities into account and derate operating voltage appropriately when a practical circuit is designed.

- a. The operating voltage of tantalum capacitors used in low impedance circuits, such as filters for power supplies (particularly switching power supplies), should be derated to less than one-third of rated voltage. In other case, keep the operating voltage below two thirds of rated voltage. Refer to **Fig.7.5-1** for detail:

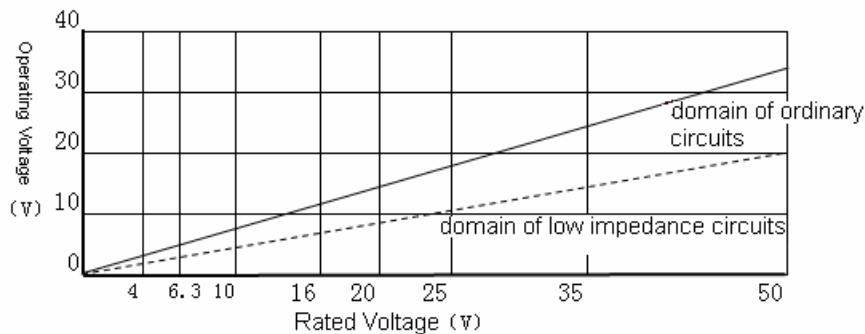


Fig.7.5-1

- b. In low impedance circuits, connecting capacitors in parallel will increase the risk of the failure caused by DC surge current. Please pay attention to the electric charge in capacitor with parallel connection which can be discharged by other capacitors.
- c. Connecting a resistor in series with capacitor is suggested to alleviate the shock caused by excessive momentary current. Please connect a protecting resistor of 3Ω/V or higher in series with the capacitor to keep current below 300mA. If protecting resistors could not be applied; please make sure operating voltage is below one-third of rated voltage (**Fig.7.5-1**).

### 7.5.2 Reverse voltage

Since tantalum capacitor has polarity, do not apply a reverse voltage to it. Do not apply capacitor to a circuit which only has alternating current.

- ① If there is no alternation, applying a low reverse voltage which is listed below to capacitor in a short time is approved:
  - At 25°C:  $\leq 10\%U_R$  (rated voltage) or 1V (whichever is lower);
  - At 85°C:  $\leq 5\%U_R$  (rated voltage) or 0.5V (whichever is lower);
  - At 125°C: 1% of rated voltage, 0.1V for max.
- ① In principle, testing a circuit with tantalum capacitor or capacitor itself by using a resistor gear of millimeters in ignorance of polarity is forbidden.
- ② During measurement and application, if the tantalum capacitor is subjected to an undesirable reverse voltage due to carelessness, please dispose it, even if its electrical characteristics are still qualified.

### 7.5.3 Ripple voltage

Please use the capacitor within permissible ripple voltage.

- a. The sum of DC bias voltage and the maximum AC branch voltage should not exceed rated voltage during operation.
- b. The sum of negative peak AC value and DC bias voltage should not exceed the specified reverse voltage.
- c. Ripple current applied to capacitor will generate active power loss, which will raise the rate of the failure caused by heat due to self-heat generation of capacitor. Therefore, ripple current and permissible power loss must be in control.

### 7.5.4 Mounting

In mounting, if the capacitor has underwent excessive mechanical and thermal shock which may cause deterioration of electrical characteristics, open circuits and short circuits, please confirm the practical mounting conditions before usage.

## 8. Recommended Soldering Technologies

### 8.1 Reflowing Profile( Fig. 8-1):

△Preheat condition: 150 ~200°C/60~120sec.

△ Allowed time above 217°C: 60~90sec.

△ Max temp: 260°C

△ Max time at max temp: 10sec.

△ Solder paste: Sn/3.0Ag/0.5Cu

△ Allowed Reflow time: 2x max

[Note: The reflow profile in the above table is only for qualification and is not meant to specify board assembly profiles. Actual board assembly profiles must be based on the customer's specific board design, solder paste and process, and should not exceed the parameters as the Reflow profile shows.]

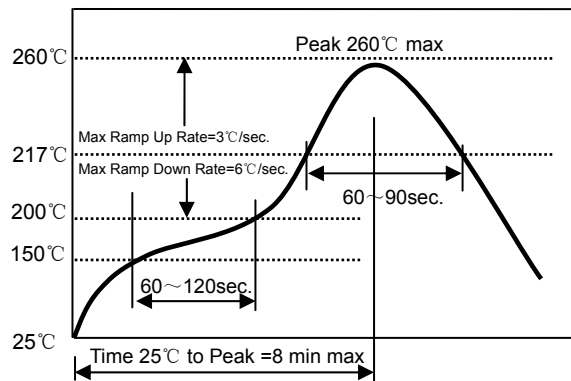


Fig. 8-1

### 8.2 Iron Soldering Profile (Fig. 8-2):

1. Iron soldering power: Max.30W
2. Pre-heating: 150 °C/60sec.
3. Soldering Tip temperature: 350°C Max.
4. Soldering time: 3sec. Max.
5. Solder paste: Sn/3.0Ag/0.5Cu
6. Max.1 times for iron soldering

[Note: Take care not to apply the tip of the soldering iron to the terminal electrodes.]

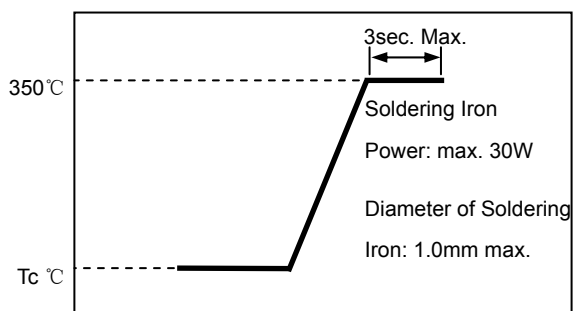


Fig. 8-2

## 9. Supplier Information

1. Supplier:  
**Shenzhen Sunlord Electronics Co., Ltd.**
- b) Manufacturer:  
**Shenzhen Sunlord Electronics Co., Ltd.**
- c) Manufacturing Address:  
Sunlord Industrial Park, Dafuyuan Industrial Zone, Guanlan, Shenzhen, China  
**Zip: 518110**