Dual P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 60m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 90m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

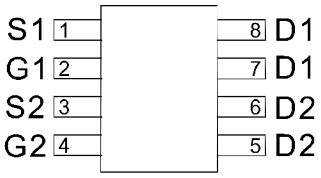
APPLICATIONS

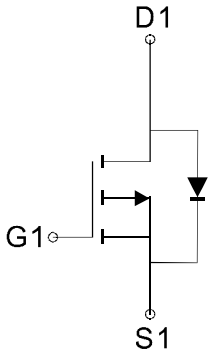
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

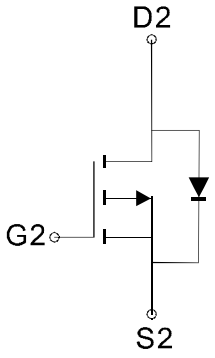
(SOP-8)

Top View





P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V_{DSS}	-30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	-5.3		A
	T_A=70℃		-4.3		
Pulsed Drain Current		I_{DM}	-30		A
Continuous Source Current (Diode Conduction)		I_S	-1.7		A
Maximum Power Dissipation	T_A=25℃	P_D	2.0		W
	T_A=70℃		1.3		
Operating Junction Temperature		T_J	-55 to 150		℃
Storage Temperature Range		T_{stg}	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	47	℃/W
			Steady State	75	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	45		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Dual P-Channel 30V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.4	-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
		V_{DS}=-30V, V_{GS}=0V T_J=55℃			-25	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -5.3A		50	60	mΩ
		V_{GS}=-4.5V, I_D= -4.2A		69	90	
V_{SD}	Diode Forward Voltage	I_S=-1.7A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		3.5		Ω
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		450	490	pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			20		
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-5.3A		14	17	nC
Qgs	Gate-Source Charge			4		
Qgd	Gate-Drain Charge			3		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω I_D=-1.0A, V_{GEN}=-10V R_G=6Ω		27	33	ns
tr	Turn-On Rise Time			11	15	
$t_{d(off)}$	Turn-Off Delay Time			40	52	
tf	Turn-Off Fall Time			4	6	

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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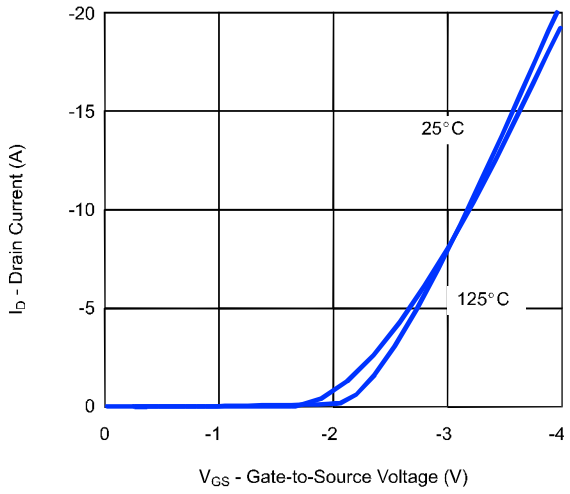
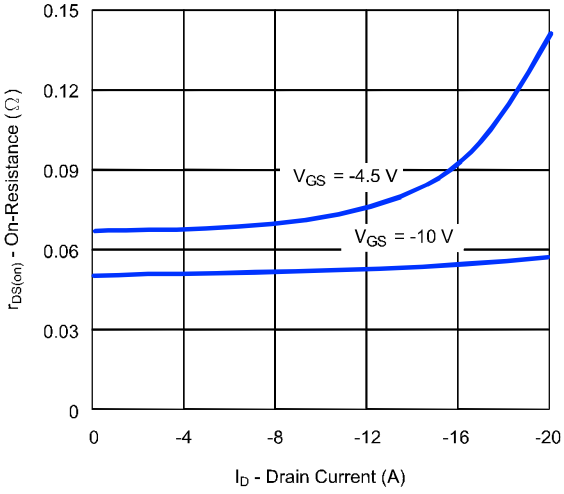
Typical Characteristics (T_J =25℃ Noted)

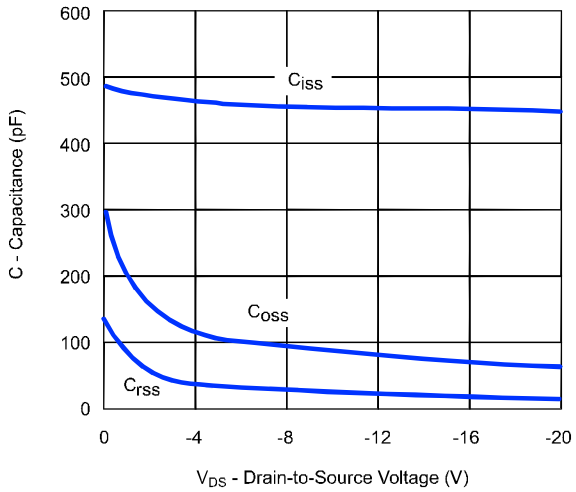
Transfer Characteristics



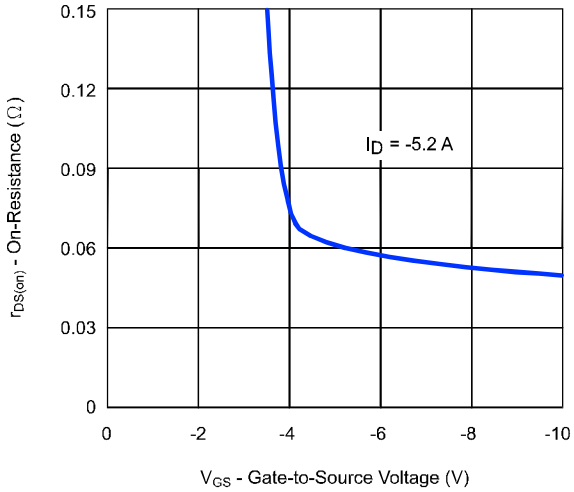
On-Resistance vs. Drain Current



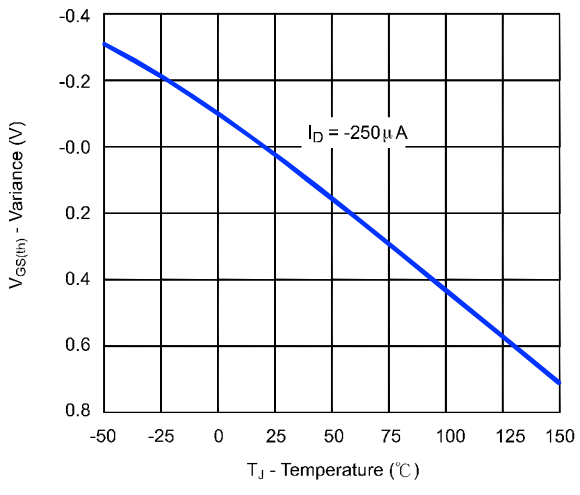
Capacitance



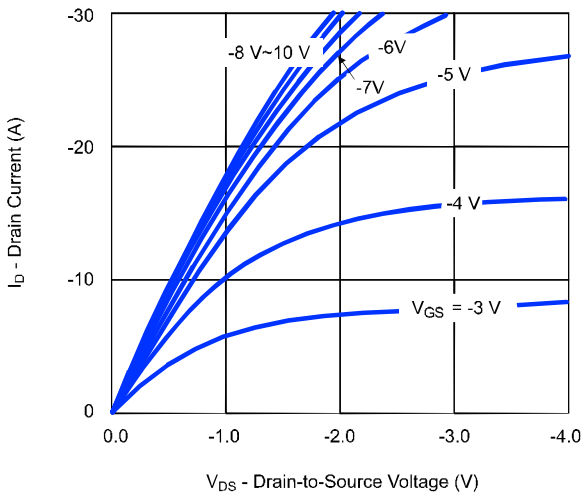
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



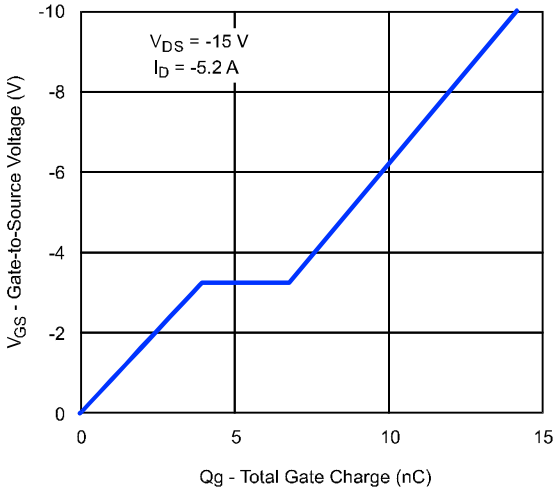
On-Region Characteristics



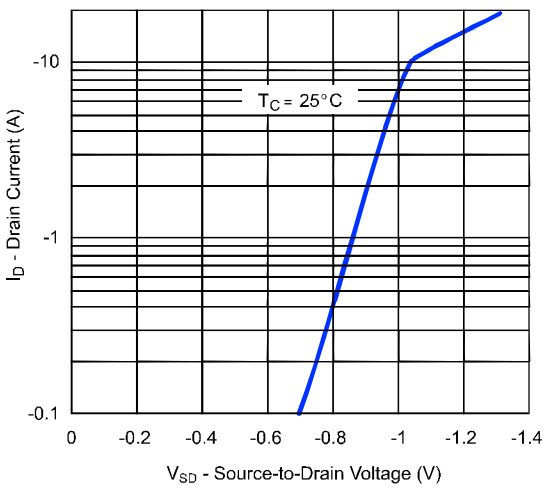
Dual P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

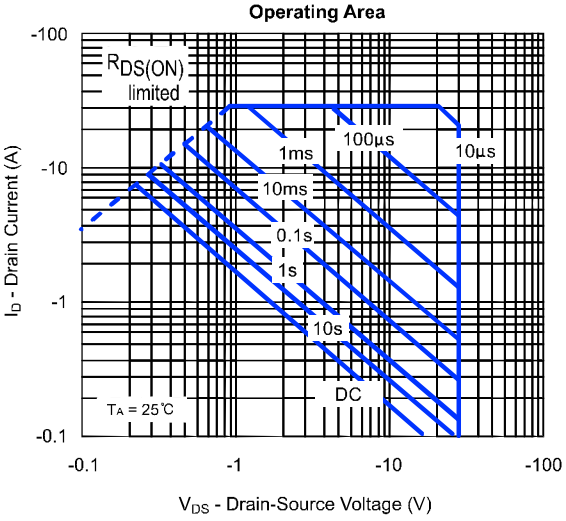
Gate Charge



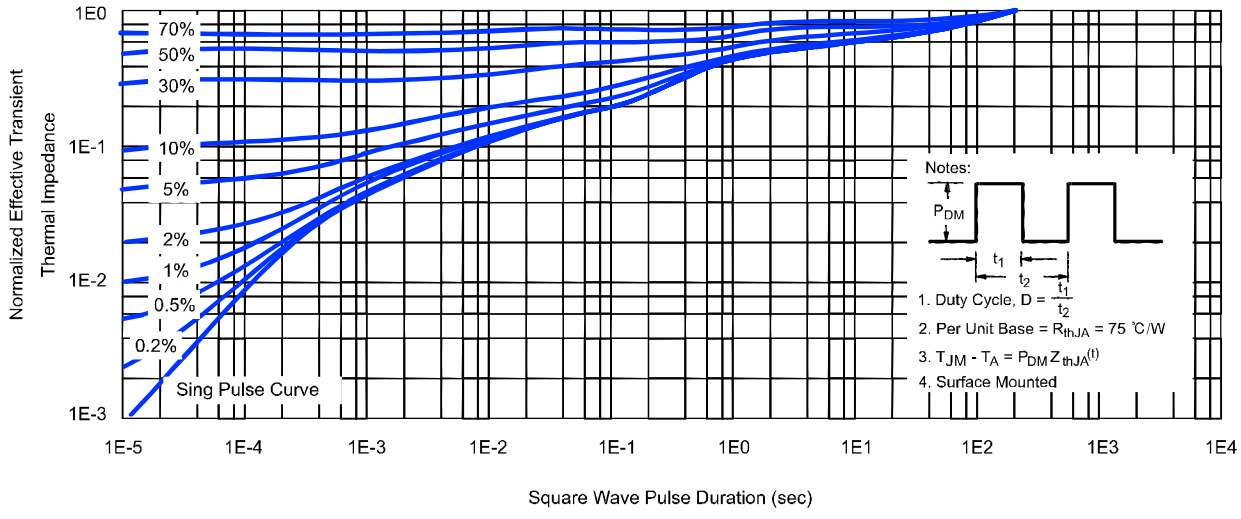
On-Resistance vs. Drain Current



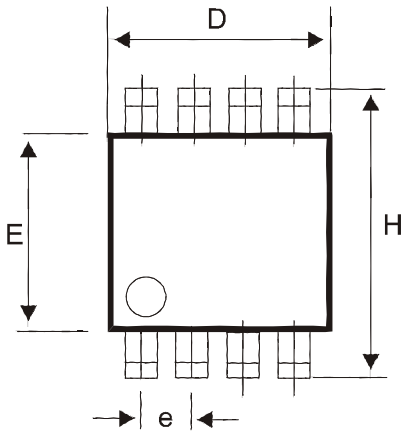
Maximum Forward Biased Safe Operating Area

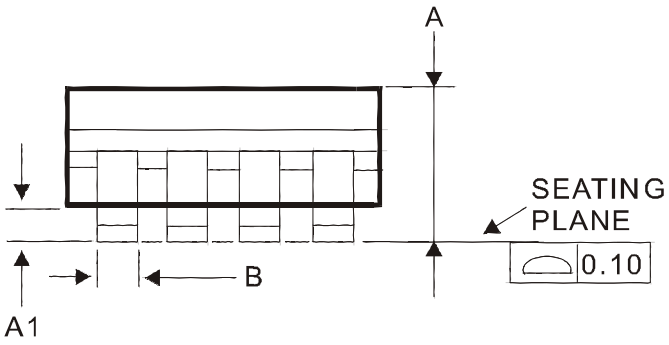


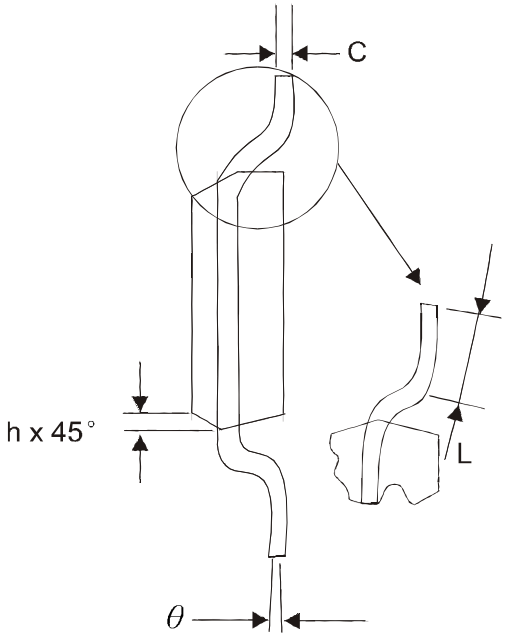
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.