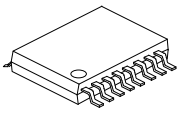
L8400 **LINEAR INTEGRATED CIRCUIT**

# FET BIAS CONTROLLER



SSOP-16(150mil)

## ■ DESCRIPTION

The UTC **L8400** is designed to bias the MOSFETs that are commonly used in LNBs that can implies minimum external components requires.

## ■ FEATURES

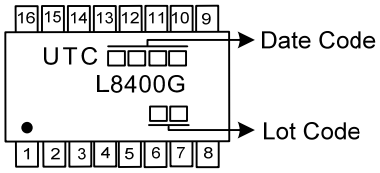
* Can Bias up to 4 FETs
* Drain Current Adjustable by Two External Resistors.
* Two Sets of Drain Current can be Setted.

## ■ ORDERING INFORMATION

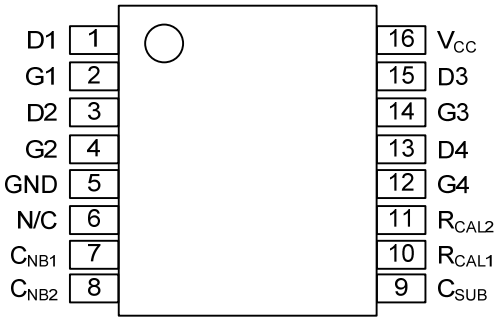
| Ordering Number | Package | Packing |
|---|---|---|
| L8400G-R16-R | SSOP-16 | Tape Reel |
| L8400G-R16-T | SSOP-16 | Tube |

| | |
|---|---|
| L8400G-R16-T<br>(1)Packing Type<br>(2)Package Type<br>(3)Green Package | (1) T: Tube, R: Tape Reel<br>(2) R16: SSOP-16<br>(3) G: Halogen Free and Lead Free |

## ■ MARKING



## ■ PIN CONFIGURATION




## ■ FUNCTIONAL DIAGRAM

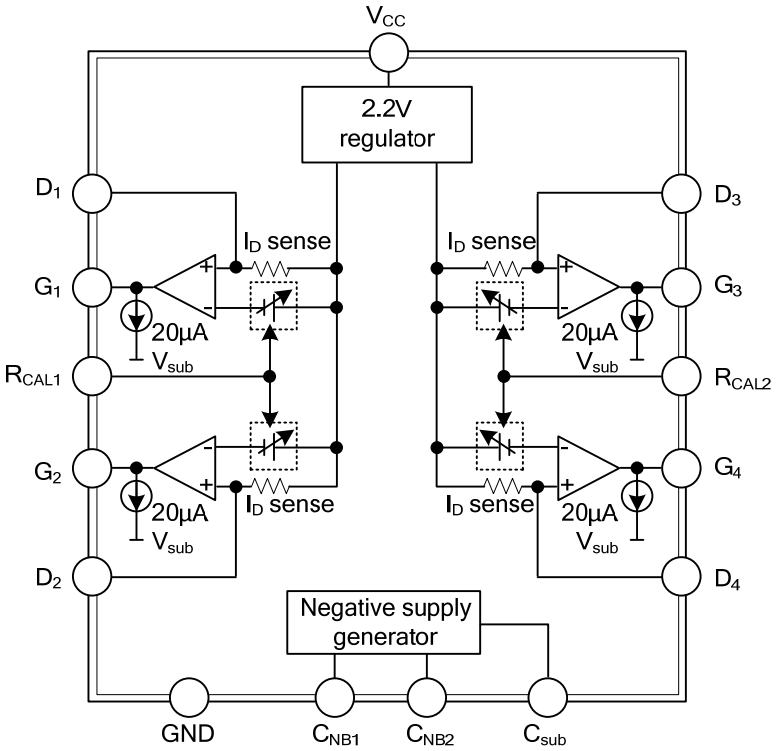



Fig.1

## ■ FUNCTIONAL DESCRIPTION

The UTC **L8400** includes one negative supply required for gate biasing from the single supply voltage, and all the other bias requirements for external FETs. As fig.1

A low current negative supply voltage includes an internal OSC and two 47nF external cap. The negative rail generator is common to all devices. This negative supply voltage used to drive the FET's gate to obtain the required drain current because of he FET is a depletion mode transistor.

There are for stages in the IC to baising the four external FETS. The drain voltage of the external FET FET1~4 is 2.2 volts set by the UTC **L8400**.

The drain current of external FET is determined by the external resist $R_{CAL1}$ or $R_{CAL2}$. External resistor $R_{CAL1}$ sets the drain current of FET1 and FET 2, and resistor $R_{CAL2}$ sets the drain current of FET3 and FET4.

## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.6 ~ 15 | V |
| Supply Current | $I_{CC}$ | 100 | mA |
| Drain Current (per FET)(set by $R_{CAL1}$ and $R_{CAL2}$) | $I_D$ | 0 ~ 15 | mA |
| Output Current | Io | 100 | mA |
| Power Dissipation($T_A$=25℃) | $P_D$ | 500 | mW |
| Operating Temperature | $T_{OPR}$ | -40 ~ +70 | °C |
| Storage Temperature | $T_{STG}$ | -50 ~ +85 | °C |

## ■ ELECTRICAL CHARACTERISTICS

($T_A$=25°C, $V_{CC}$=5V, $I_D$=10mA, $R_{CAL1}$= $R_{CAL2}$ =33KΩ, unless otherwise specified.)

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | | 5 | | 12 | V |
| Supply Current | | $I_{CC}$ | $I_{D1}$ to $I_{D4}$=0 | | | 15 | mA |
| | | | $I_{D1}$ to $I_{D4}$=10mA | | | 75 | |
| Substrate Voltage (Internally generated) | | $V_{SUB}$ | $I_{SUB}$ =0 | -3.5 | -3 | -2 | V |
| | | | $I_{SUB}$ = -200μA | | | -2 | |
| Output Noise | Gate Voltage | $E_{NG}$ | $C_G$=4.7nF, $C_D$=10nF | | | 0.005 | $V_{PKPK}$ |
| | Drain Voltage | $E_{ND}$ | $C_G$=4.7nF, $C_D$=10nF | | | 0.02 | |
| Oscillator Freq. | | $f_O$ | | 200 | 350 | 800 | kHz |

## ■ GATE CHARACTERISTICS

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Current Range | | $I_{GO}$ | | -30 | | 2000 | μA |
| Output Voltage | Output Low | $V_{OL}$ | $I_{D1}$ to $I_{D4}$=12mA | -3.5 | | -2 | V |
| | | | $I_{G1}$ to $I_{G4}$=0 | | | | V |
| | | | $I_{D1}$ to $I_{D4}$=12mA | -3.5 | | -2 | V |
| | | | $I_{G1}$ to $I_{G4}$= -10μA | | | | V |
| | Output High | $V_{OH}$ | $I_{D1}$ to $I_{D4}$=8mA | 0 | | 1 | V |
| | | | $I_{G1}$ to $I_{G4}$=0 | | | | V |

Note: Noise voltage measurement would be ignored in production.

## ■ DRAIN CHARACTERISTICS

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Current | | $I_D$ | | 8 | 10 | 12 | mA |
| Current Change | With $V_{CC}$ | $\triangle I_{DV}$ | $V_{CC}$=5 ~ 12V | | 0.02 | | %/V |
| | With $T_J$ | $\triangle I_{DT}$ | $T_J$=-40 ~ +70℃ | | 0.05 | | %/℃ |
| Voltage | | $V_D$ | | 2 | 2.2 | 2.4 | V |
| Voltage Change | With $V_{CC}$ | $\triangle V_{DV}$ | $V_{CC}$=5 ~ 12V | | 0.5 | | %/V |
| | With $T_J$ | $\triangle V_{DT}$ | $T_J$=-40 ~ +70℃ | | 50 | | ppm |

## ■ TYPICAL APPLICATION CIRCUIT

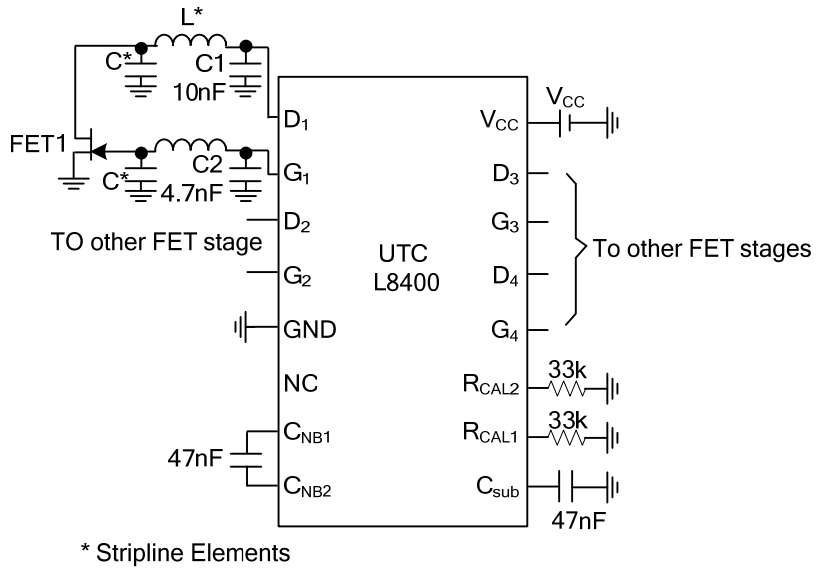



Fig.2

## ■ APPLICATIONS INFORMATION

It is application circuit of UTC **L8400** in figure 2, the bias circuits is stable fully in -40°C ~70°C.

CNB and $C_{SUB}$ are used to generated the negative supply on pin $C_{SUB}$ (about -3V), which can be used to power other external circuits, but it is low load current is noticeable.

C1 and C2 are used to suppress noise or RF interference in each stage of the IC or other external circuits in application circiut system. Value of C1 and C2 could be used in 1nF to 100nF as design dependent.

$R_{CAL1}$ and $R_{CAL2}$ are used to set the drain current of FETs 1 & 2 and FETS 3 & 4. If the same drain current is required for all FETs on UTC **L8400**, then the pin $R_{CAL1}$ and $R_{CAL2}$ can be connected to GND through only one res of half normal value.

There are full protection for external FETs on chip: The gate output voltage is limitted in -3.5V~0.7V in any conditions including powerup and powerdown transients; If the negative bias generator be shorted or overloaded, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

The fig.3 is typical applications of UTC **L8400** in LNB.

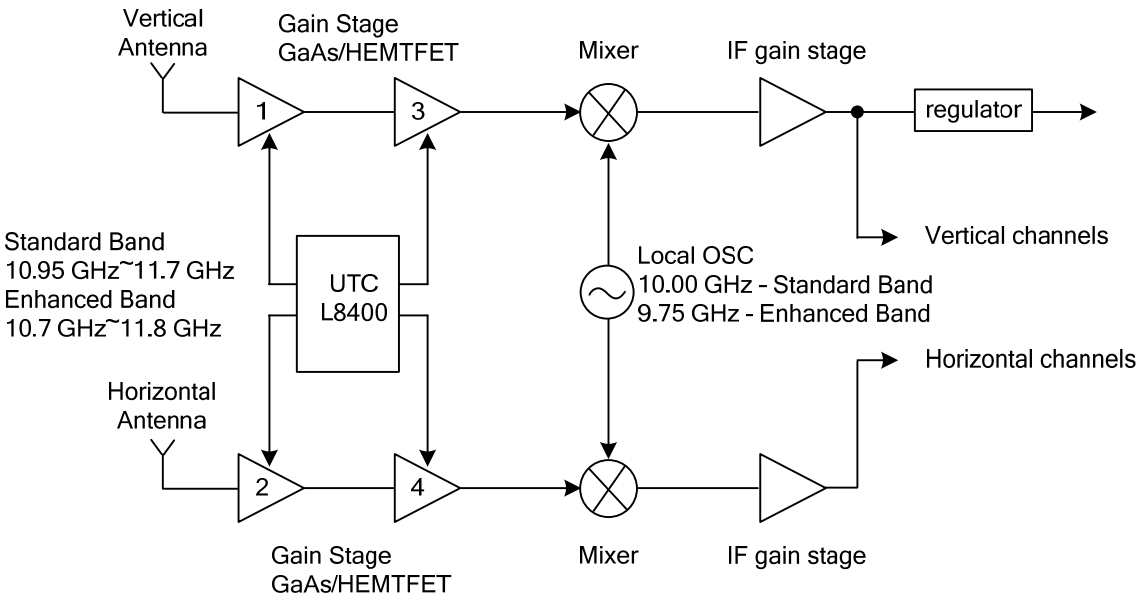
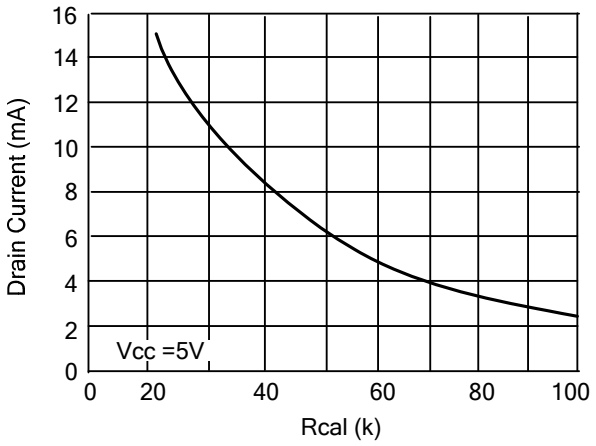


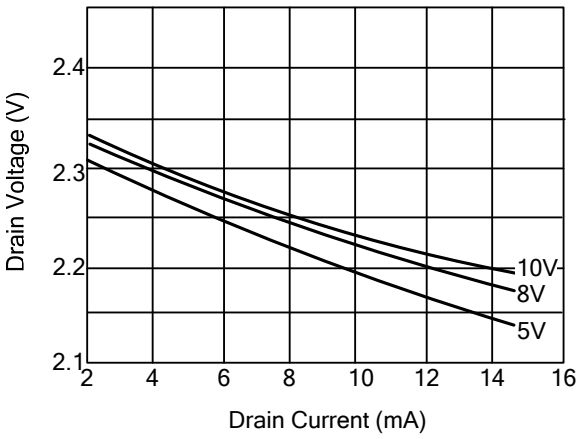

Fig.3

## ■ TYPICAL CHARACTERISTICS

JFET Drain Current vs Rcal




JFET Drain Voltage vs Drain Current




Vsub vs External Load