TLVx333 2μV V_{OS}、0.02μV/°C、17μA、CMOS 运算放大器零漂移系列

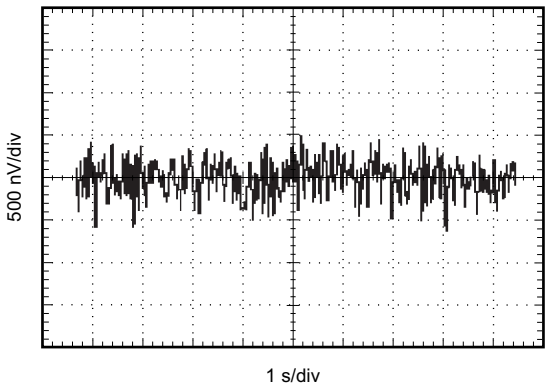
1 特性

- 无与伦比的性价比
- 低偏移电压：2μV
- 零点漂移：0.02μV/°C
- 低噪声：1.1 μV_{PP}，0.1Hz 至 10Hz
- 静态电流：17μA
- 电源电压：1.8V 至 5.5V
- 轨到轨输入/输出
- 内部电磁干扰 (EMI) 滤波功能
- 微型封装：SOT23、SC70

2 应用

- 电池供电仪器
- 温度测量
- 变频器应用
- 电子称
- 医疗仪表
- 手持测试设备
- 电流感测

0.1Hz 至 10Hz 噪声



3 说明

TLVx333 系列 CMOS 运算放大器不但具备精密的性能，而且价格极具竞争力。这些器件属于采用专有自动校准技术的零漂移系列放大器，在整个时间和温度范围内的偏移电压非常低（最大 15μV）且几乎零漂移，并且静态电流只有 28μA。TLVx333 系列放大器具有轨到轨输入/输出以及几乎不变的 1/f 噪声特性，因此是许多应用的理想选择，更容易设计到系统中。这些器件经过优化，适合在 1.8V (±0.9V) 至 5.5V (±2.75V) 的低压状态下工作。

TLV333（单通道版本）提供 SC70-5、SOT23-5 和 SOIC-8 三种封装。TLV2333（双通道版本）提供 VSSOP-8 和 SOIC-8 两种封装。TLV4333 提供标准 SOIC-14 和 TSSOP-14 两种封装。所有器件版本的额定工作温度范围均为 -40°C 至 +125°C。

器件信息(1)

部件号	封装	封装尺寸（标称值）
TLV333	SOIC (8)	4.90mm x 3.91mm
	SOT-23 (5)	2.90mm x 1.60mm
	SC70 (5)	2.00mm × 1.25mm
TLV2333	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
TLV4333	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

目录

4 修订历史记录

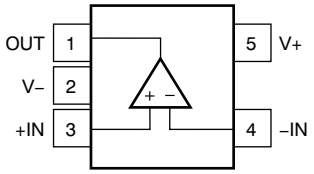
日期	修订版本	注释
2015 年 12 月	*	最初发布版本。

5 Device Comparison Table

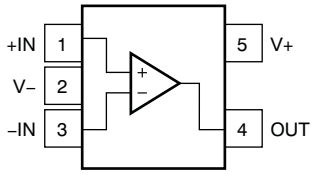
DEVICE	NO. OF CHANNELS	PACKAGE-LEADS				
		SOIC	SOT23	SC70	VSSOP	TSSOP
TLV333	1	8	5	5	—	—
TLV2333	2	8	—	—	8	—
TLV4333	4	14	—	—	—	14

6 Pin Configuration and Functions

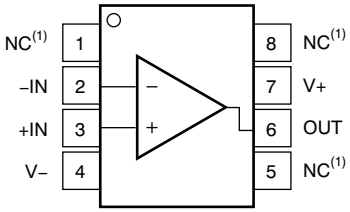
DBV Package: TLV333
5-Pin SOT23
Top View



DCK Package: TLV333
5-Pin SC70
Top View



D Package: TLV333
8-Pin SOIC
Top View

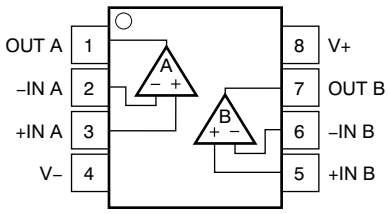


(1) NC denotes no internal connection.

Pin Functions: TLV333

NAME	PIN NO.			I/O	DESCRIPTION
	DBV (SOT23)	DCK (SC70)	D (SOIC)		
–IN	4	3	2	I	Inverting input
+IN	3	1	3	I	Noninverting input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	4	6	O	Output
V–	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

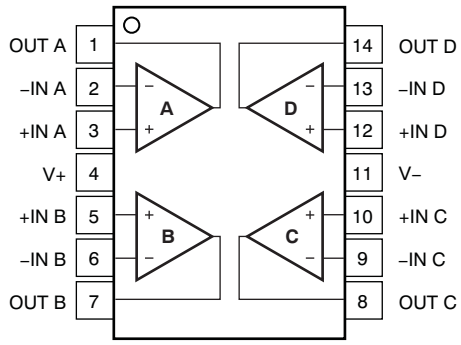
D Package: TLV2333
8-Pin SOIC, VSSOP
Top View



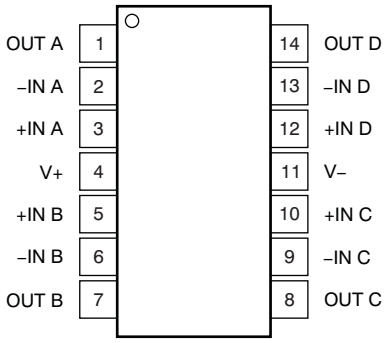
Pin Functions: TLV2333

PIN		I/O	DESCRIPTION
NAME	NO.		
	D (SOIC, VSSOP)		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

D Package: TLV4333
14-Pin SOIC
Top View



PW Package: TLV4333
14-Pin TSSOP
Top View



Pin Functions: TLV4333

PIN			I/O	DESCRIPTION
NAME	NO.			
	D (SOIC)	PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
–IN C	9	9	I	Inverting input, channel C
+IN C	10	10	I	Noninverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		7	V
Signal input pins(2)	Voltage	(V–) –0.3	(V+) + 0.3	V
	Current	–10	10	mA
Output short-circuit(3)		Continuous		
Temperature	Operating	–40	150	°C
	Junction		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8		5.5	V
	Specified temperature range	–40		125	°C

7.4 Thermal Information: TLV333

THERMAL METRIC(1)		TLV333			UNIT
		D (SOIC)	DBV (SOT23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information: TLV2333

THERMAL METRIC(1)		TLV2333		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information: TLV4333

THERMAL METRIC(1)		TLV4333		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	120.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	56.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.7 Electrical Characteristics: V_S = 1.8 V to 5.5 V

at T_A = 25°C, R_L = 10 kΩ connected to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage (1)	V_S = 5 V		2	15	µV
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to +125°C		0.02		µV/°C
PSRR	V_{OS} vs power supply	V_S = 1.8 V to 5.5 V		1	8	µV/V
	Long-term stability (2)			1 (2)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±70		pA
	Input bias current over temperature	T_A = –40°C to +125°C		±150		pA
I_{OS}	Input offset current			±140		pA
NOISE						
e_n	Input voltage noise density	f = 1 kHz		55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		
i_n	Input current noise	f = 10 Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	102	115		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.1 V< V_O < (V+) – 0.1 V	102	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = 1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	T_A = –40°C to +125°C		30	70	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive		See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 350 kHz, I_O = 0 mA		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, T_A = –40°C to +125°C		17	28	µA
	Turn-on time	V_S = 5 V		100		µs
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C
	Storage range		–65		150	°C

(1) Specified by design and characterization. Amplifiers are 100% production screened at 25°C to reduce defective units.
(2) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

7.8 Typical Characteristics

at T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

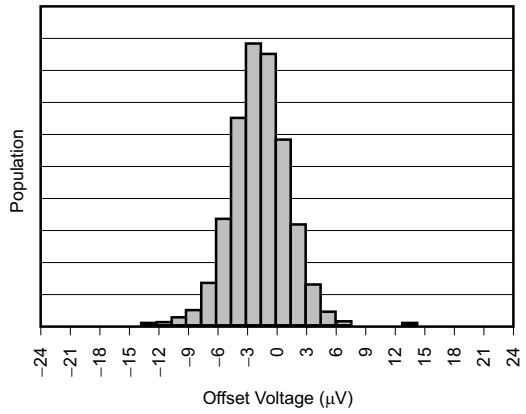


Figure 1. Offset Voltage Production Distribution

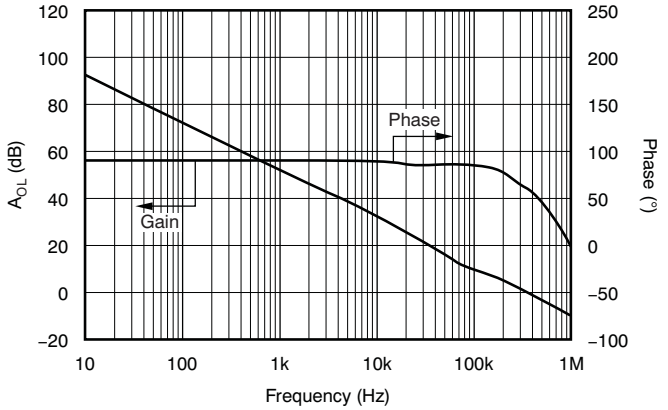


Figure 2. Open-Loop Gain vs Frequency

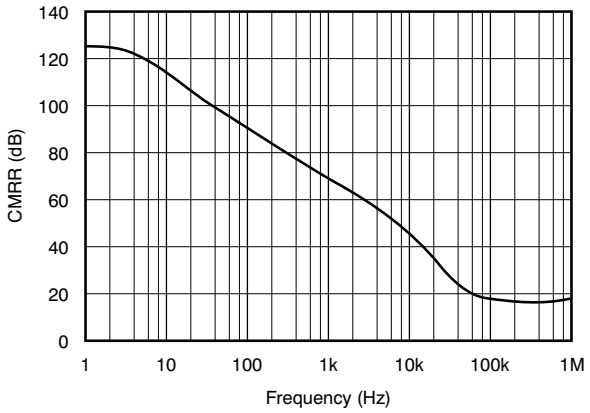


Figure 3. Common-Mode Rejection Ratio vs Frequency

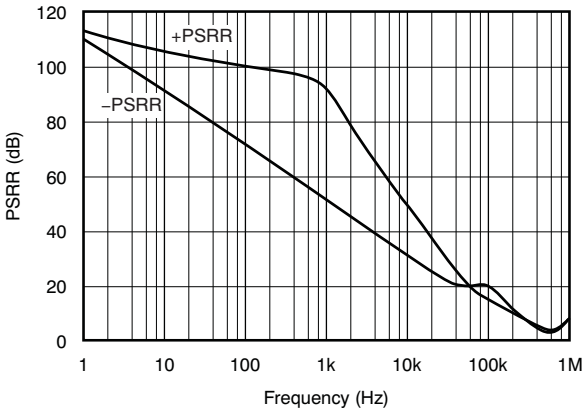


Figure 4. Power-Supply Rejection Ratio vs Frequency

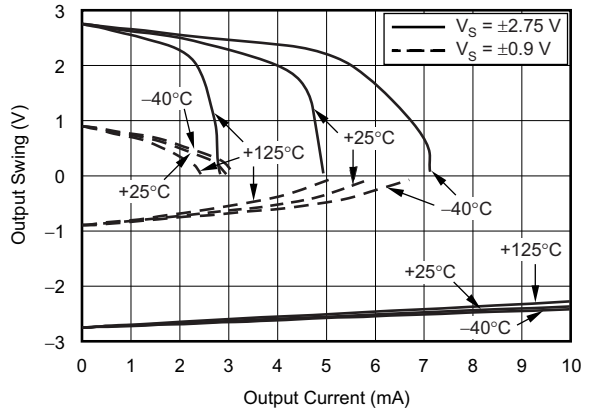


Figure 5. Output Voltage Swing vs Output Current

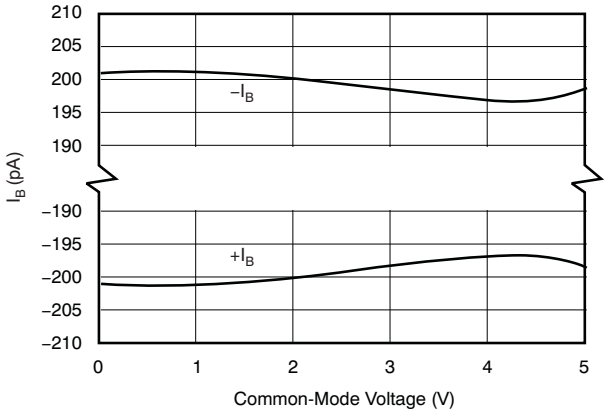


Figure 6. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

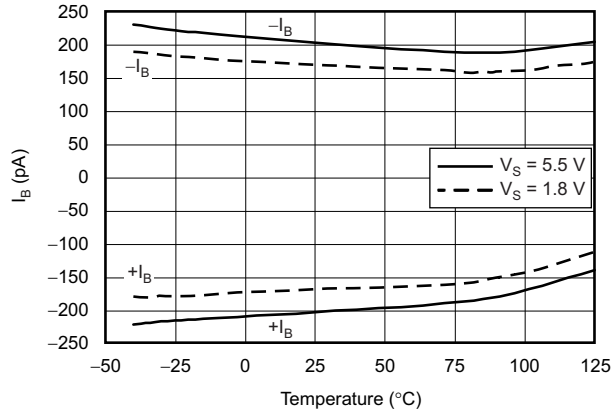


Figure 7. Input Bias Current vs Temperature

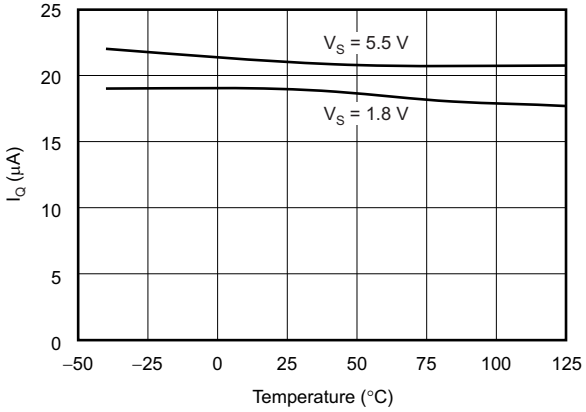
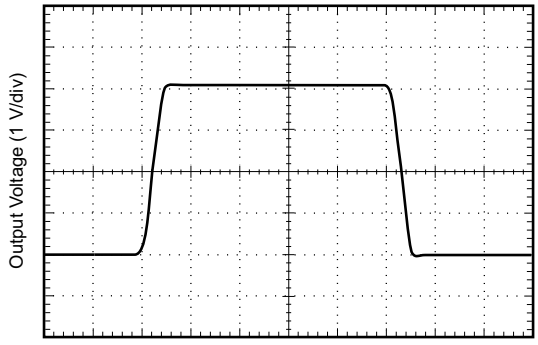
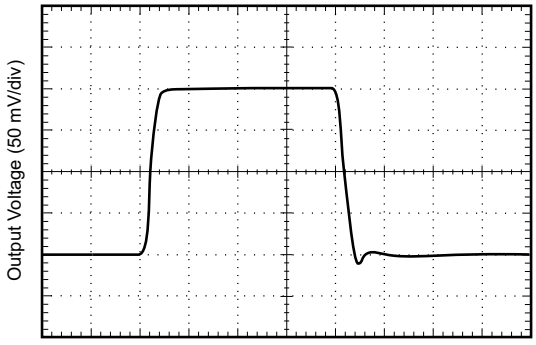


Figure 8. Quiescent Current vs Temperature



G = 1, R_L = 10 kΩ

Figure 9. Large-Signal Step Response



G = 1, R_L = 10 kΩ

Figure 10. Small-Signal Step Response

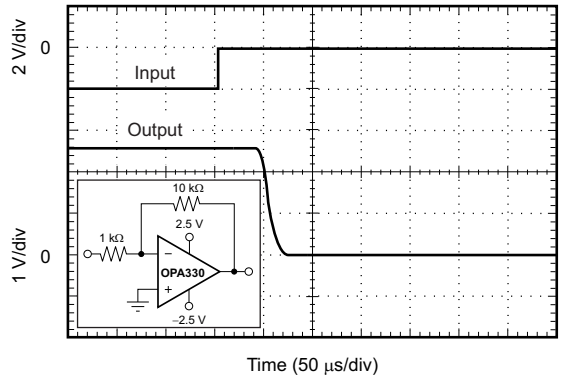


Figure 11. Positive Overvoltage Recovery

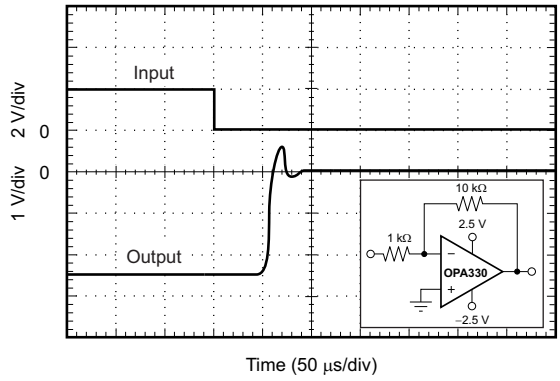


Figure 12. Negative Overvoltage Recovery

Typical Characteristics (continued)

at T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

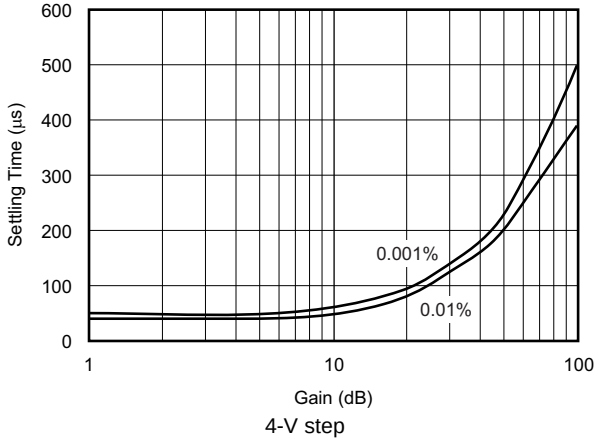


Figure 13. Settling Time vs Closed-Loop Gain

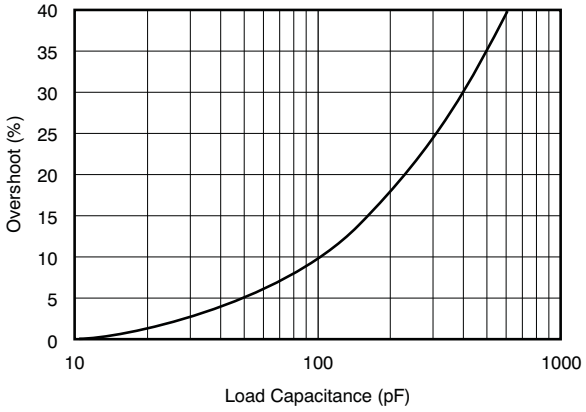


Figure 14. Small-Signal Overshoot vs Load Capacitance

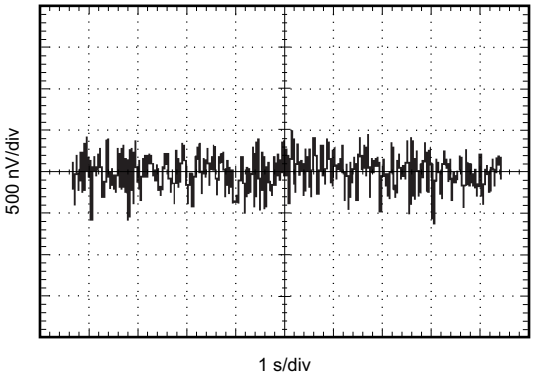


Figure 15. 0.1-Hz to 10-Hz Noise

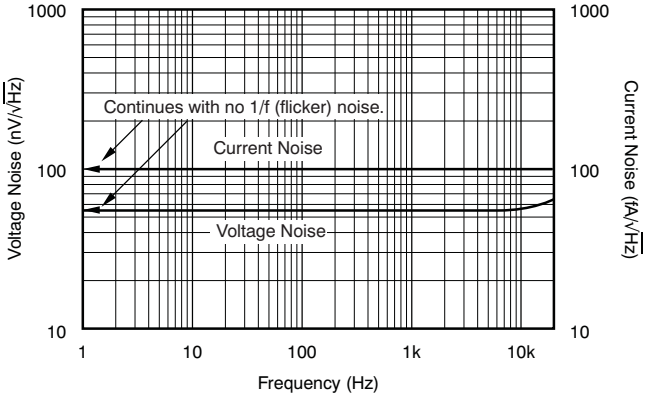


Figure 16. Current and Voltage Noise Spectral Density vs Frequency

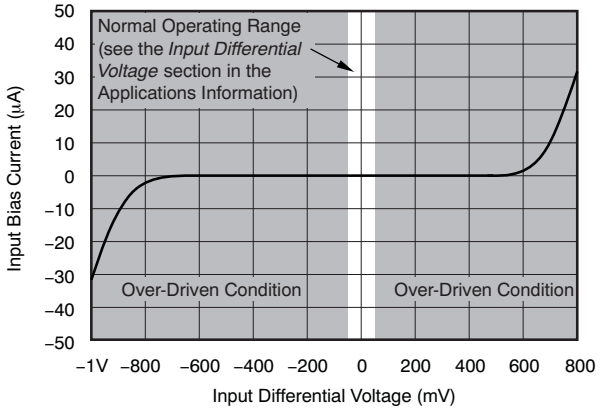


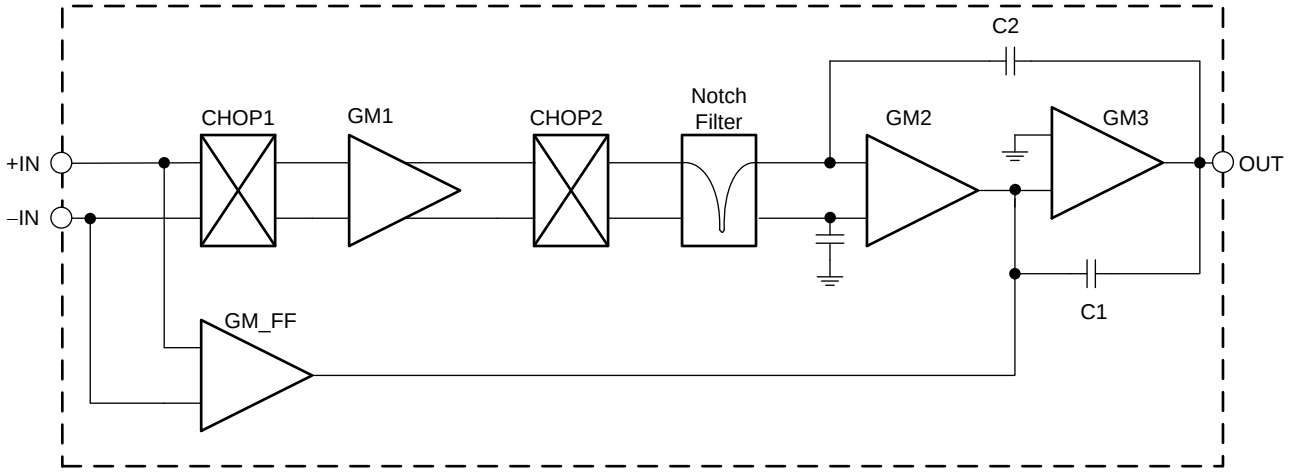
Figure 17. Input Bias Current vs Input Differential Voltage

8 Detailed Description

8.1 Overview

The TLVx333 series of low-cost operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. The TLVx333 family also offers rail-to-rail input and output and near-flat 1/f noise. These features make this series of op amps ideal for many applications and much easier to design into a wide variety of systems.

8.2 Functional Block Diagram



8.3 Feature Description

The TLV333, TLV2333, and TLV4333 are unity-gain stable, precision operational amplifiers free from unexpected output phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The TLV333 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The TLV333 series are precision amplifiers for cost-sensitive applications.

8.3.1 Operating Voltage

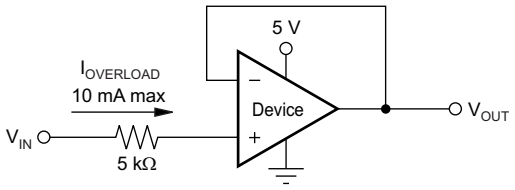
The TLV333 series op amps can be used with single or dual supplies from an operating range of V_S = 1.8 V (±0.9 V) up to 5.5 V (±2.75 V). Supply voltages greater than 7 V can permanently damage the device; see the *Absolute Maximum Ratings* table. Key parameters that vary over the supply voltage or temperature range are listed in the *Typical Characteristics* section.

Feature Description (continued)

8.3.2 Input Voltage

The TLV333, TLV2333, and TLV4333 input common-mode voltage range extends 0.1 V beyond the supply rails. The TLV333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 200 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.



NOTE: A current-limiting resistor required if the input voltage exceeds the supply rails by ≥ 0.3 V.

Figure 18. Input Current Protection

8.3.3 Internal Offset Correction

The TLV333, TLV2333, and TLV4333 op amps use an auto-calibration technique with a time-continuous, 125-kHz op amp in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp can swing close to single-supply ground, but does not reach ground. The output of the TLV333, TLV2333, and TLV4333 can be made to swing to ground, or slightly below, on a single-supply power source. This swing to ground requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. Connect a pull-down resistor between the output and the additional negative supply to pull the output down below the value that the output can otherwise achieve, as shown in Figure 19.

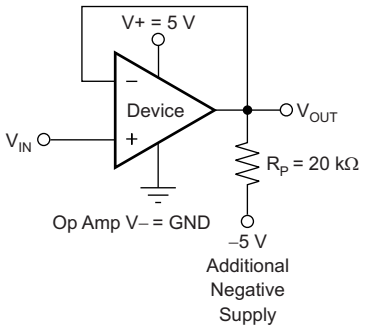


Figure 19. For V_{OUT} Range to Ground

Feature Description (continued)

The TLV333, TLV2333, and TLV4333 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The TLV333, TLV2333, and TLV4333 are characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. Note that this configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns when the output is again driven above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

8.3.5 Input Differential Voltage

The typical input bias current of the TLV333 during normal operation is approximately 200 pA. In overdriven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an overdriven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 20. Notice that the input bias current remains within specification within the linear region.

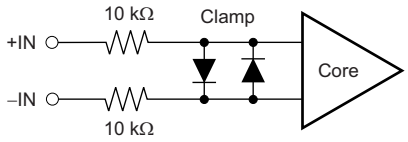


Figure 20. Equivalent Input Circuit

8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The TLV333 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a roll-off of 20 dB per decade.

8.4 Device Functional Modes

The TLV333 devices have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 System Examples

Figure 21 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 22.

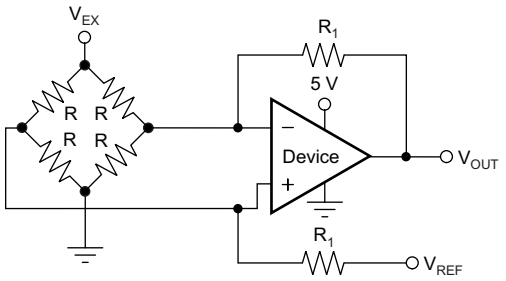
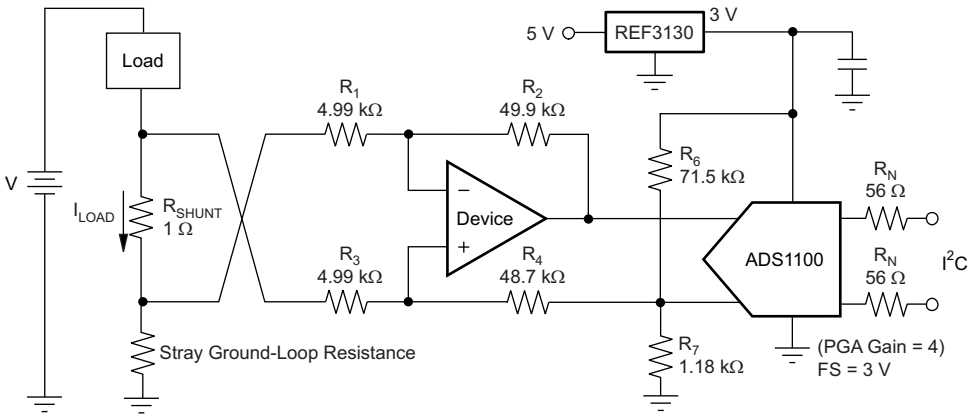


Figure 21. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 22. Low-Side Current Monitor

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

Figure 23 shows the TLV333 in a typical thermistor circuit.

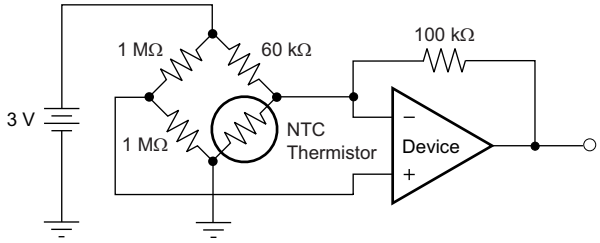


Figure 23. Thermistor Measurement

10 Power Supply Recommendations

The TLV333 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

11.1.1 General Layout Guidelines

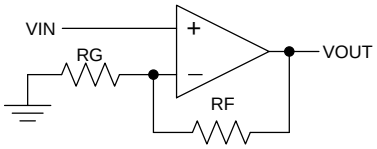
Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and to provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on materials used.

11.2 Layout Example



(Schematic Representation)

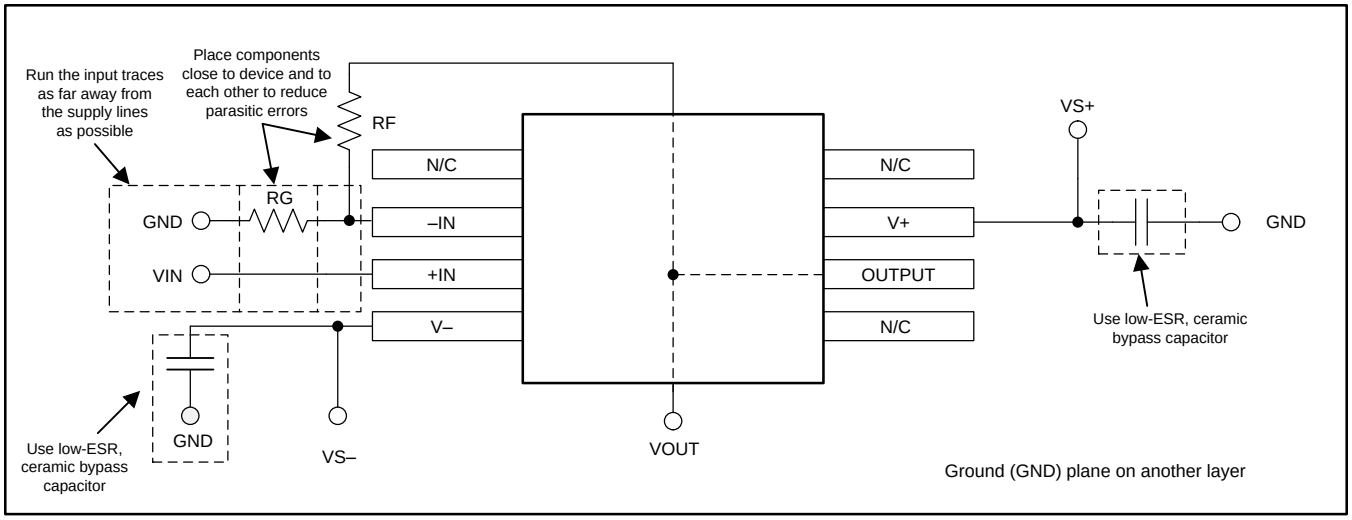


Figure 24. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

关于此产品的开发支持，请参见以下内容：

- 高侧 V-I 转换器，0V 至 2V，0mA 至 100mA，1% 满量程误差，TIPD102
- 低电平 V-I 转换器参考设计，0V 至 5V 输入，0μA 至 5μA 输出，TIPD107
- 18位、1MSPS、串行接口、微功耗、真正差分输入 SAR ADC，ADS8881
- 超低功耗、高速、轨到轨输入/输出、电压反馈运算放大器，THS4281
- 优化为最低失真、最低噪声、18 位、1MSPS 的数据采集参考设计，TIPD115
- 自校准 16 位模数转换器，ADS1100
- 最高 20ppm/℃、100μA、SOT23-3 系列电压基准，REF3130

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《QFN/SON PCB 连接》*，SLUA271
- *《四方扁平无引线逻辑器件封装》*，SCBA017

12.3 相关链接

表 1 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
TLV333	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV2333	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV4333	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
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无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2333IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12Z6	Samples
TLV2333IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12Z6	Samples
TLV2333IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV233	Samples
TLV333IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD	Samples
TLV333IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD	Samples
TLV333IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12B	Samples
TLV333IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12B	Samples
TLV333IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV333	Samples
TLV4333IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333	Samples
TLV4333IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

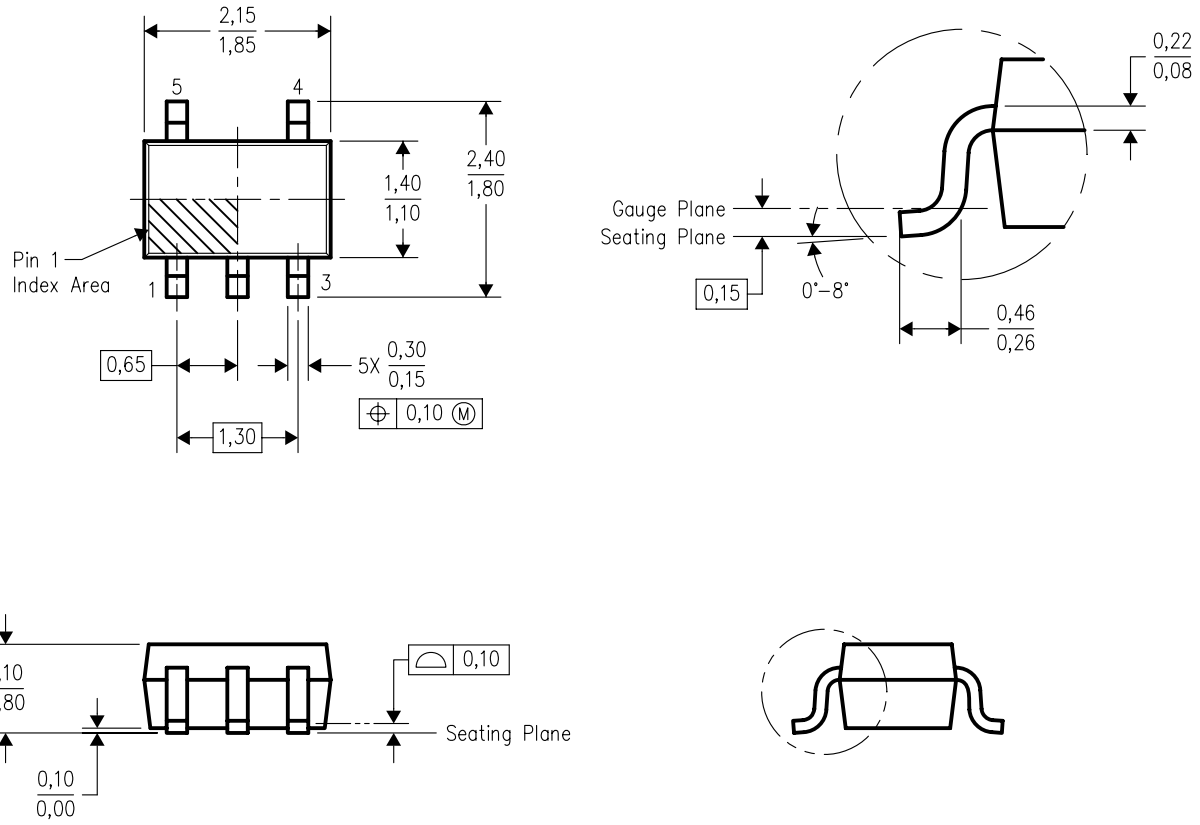
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

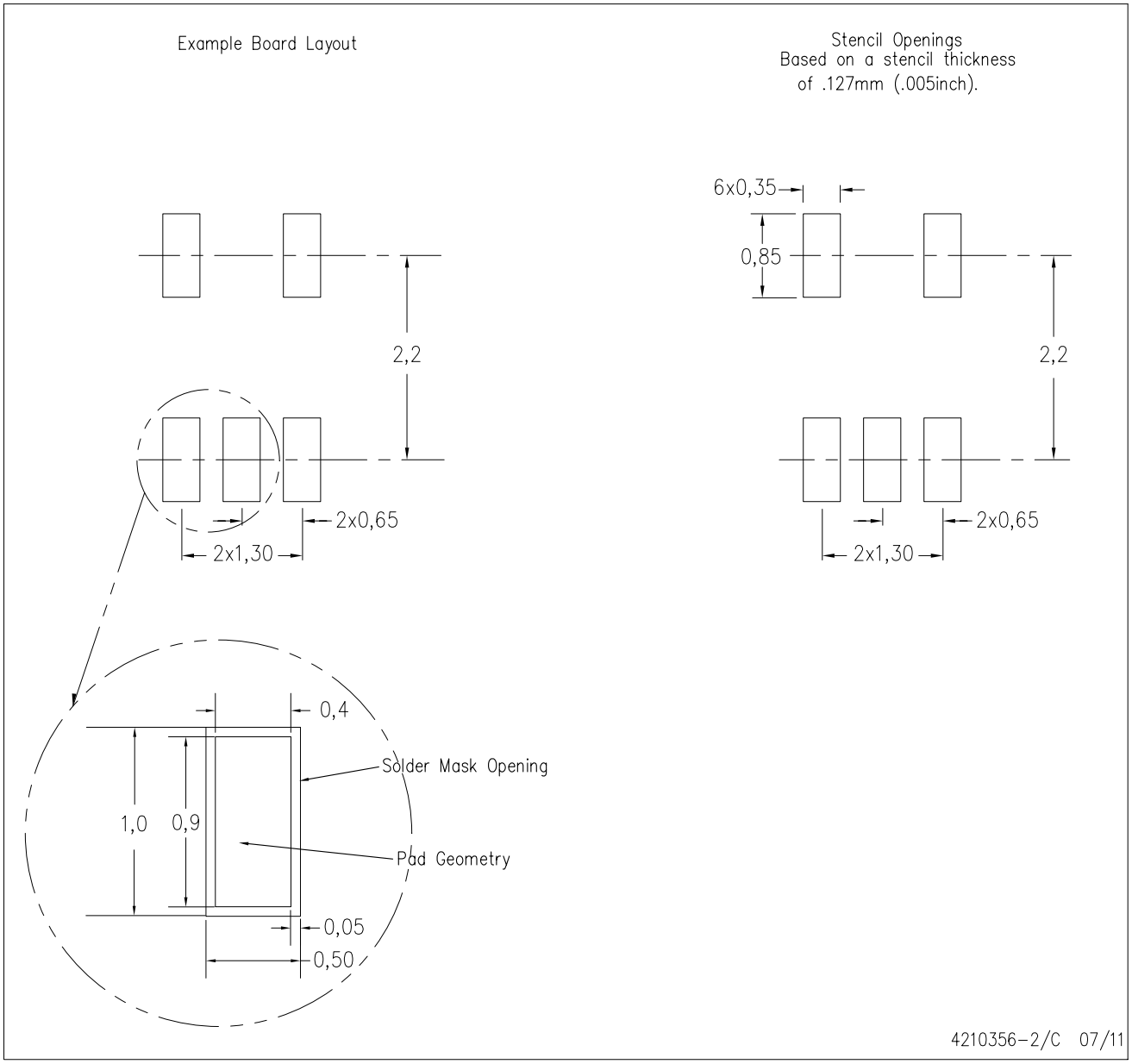
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

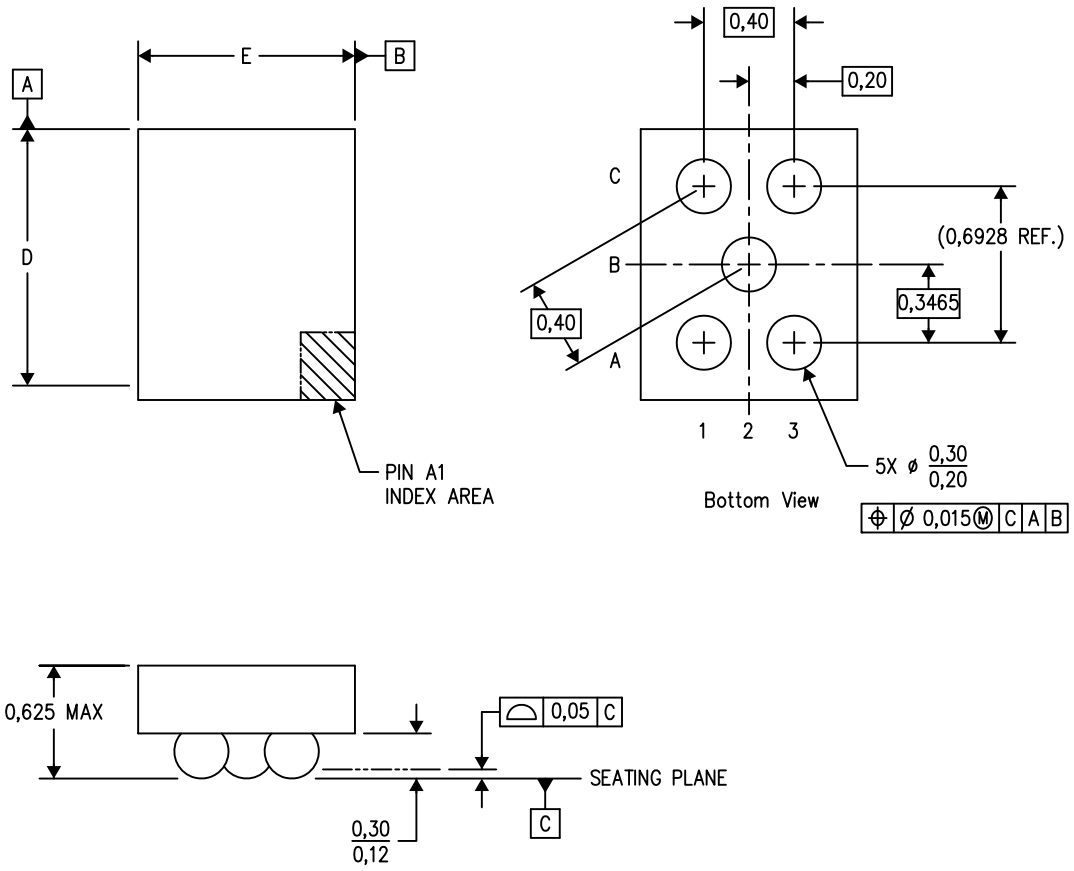
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YFF (S–XBGA–N5) DIE–SIZE BALL GRID ARRAY

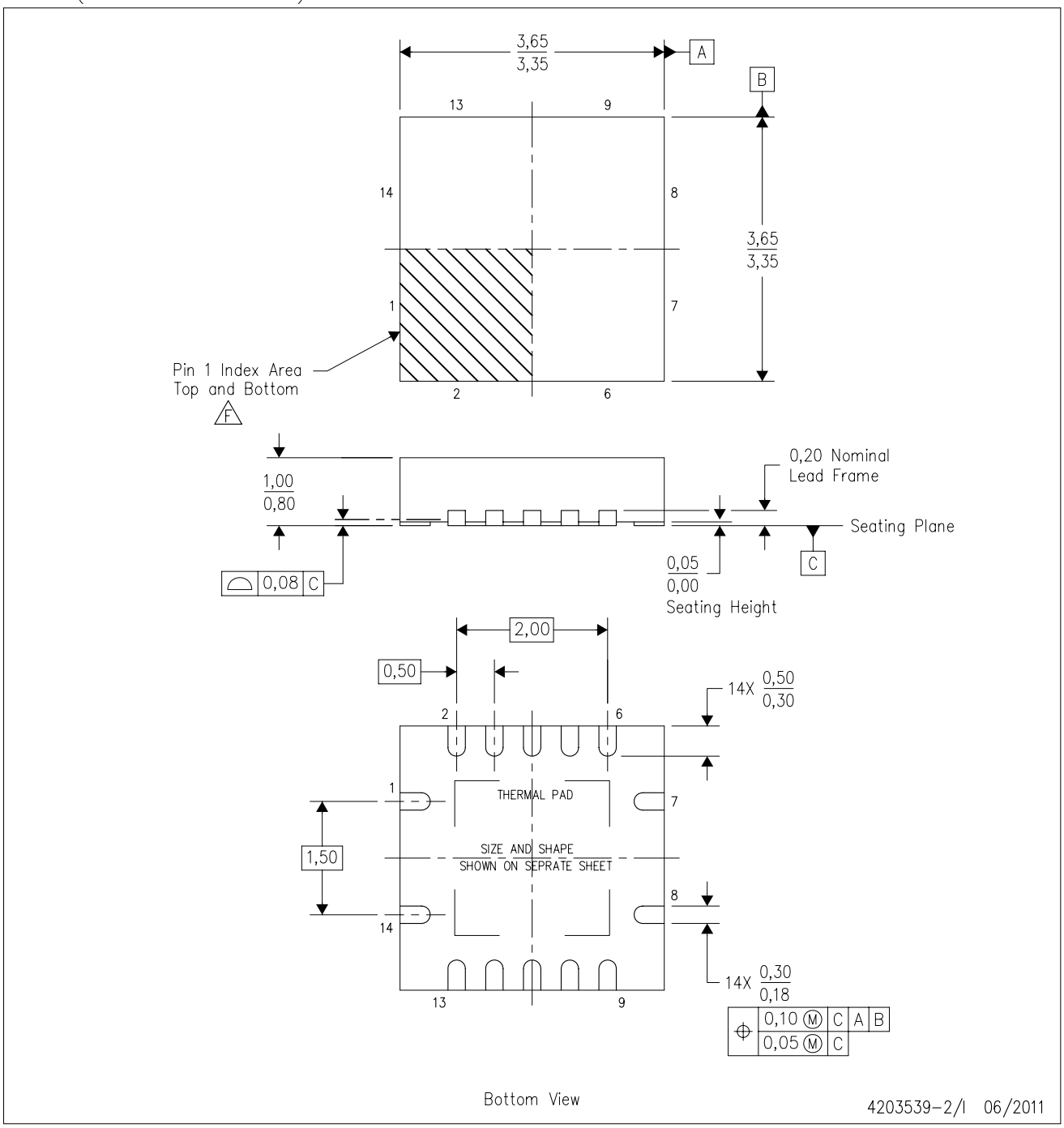


4207625–3/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

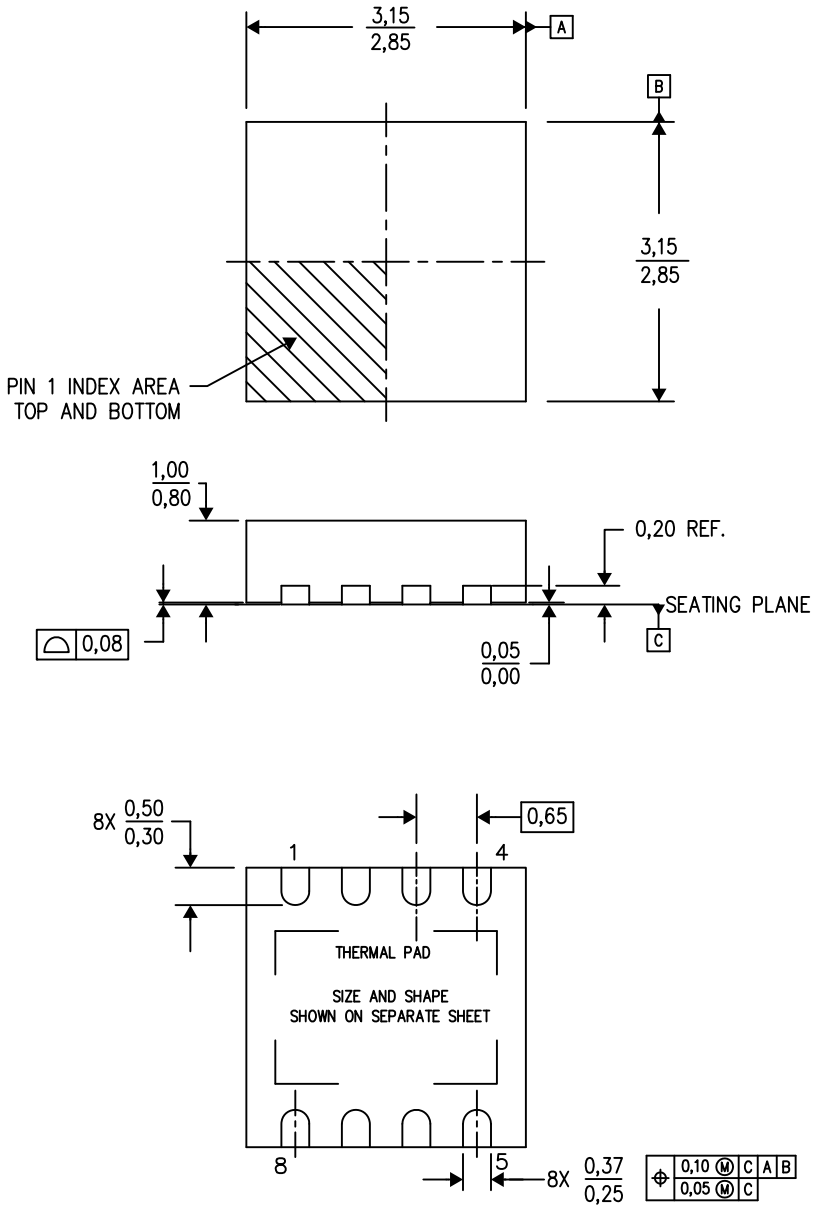
NanoFree is a trademark of Texas Instruments.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

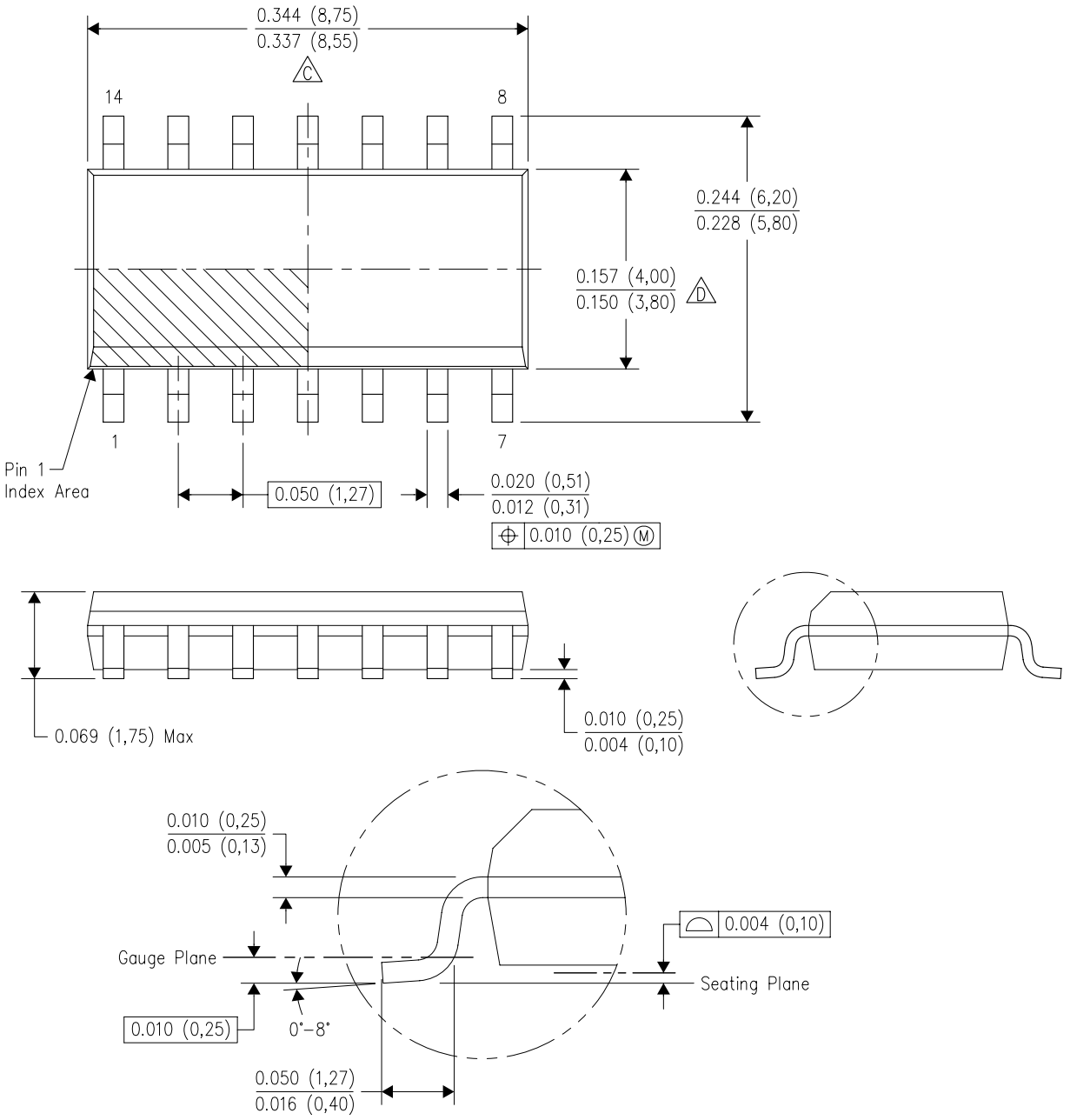
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

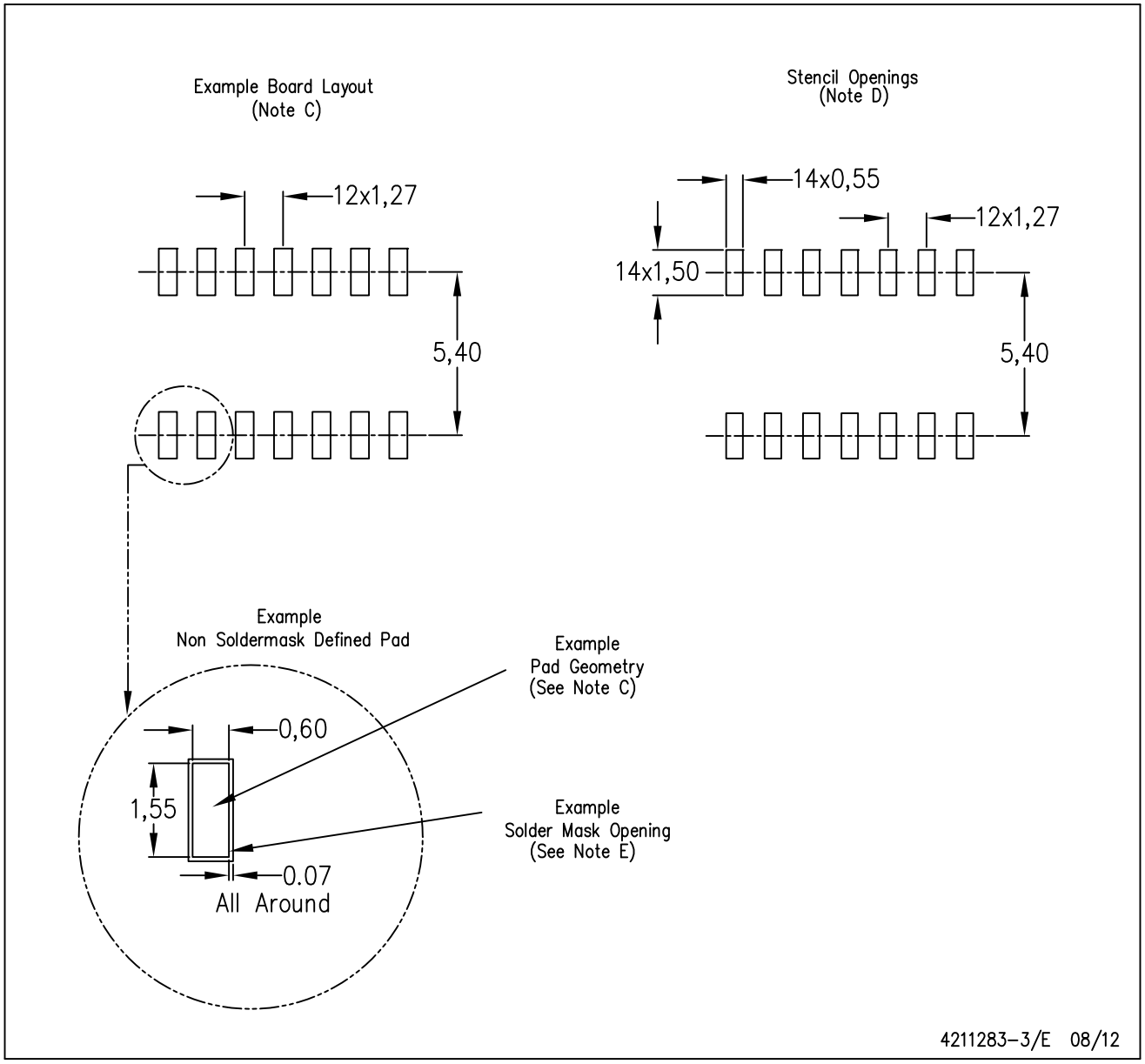
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

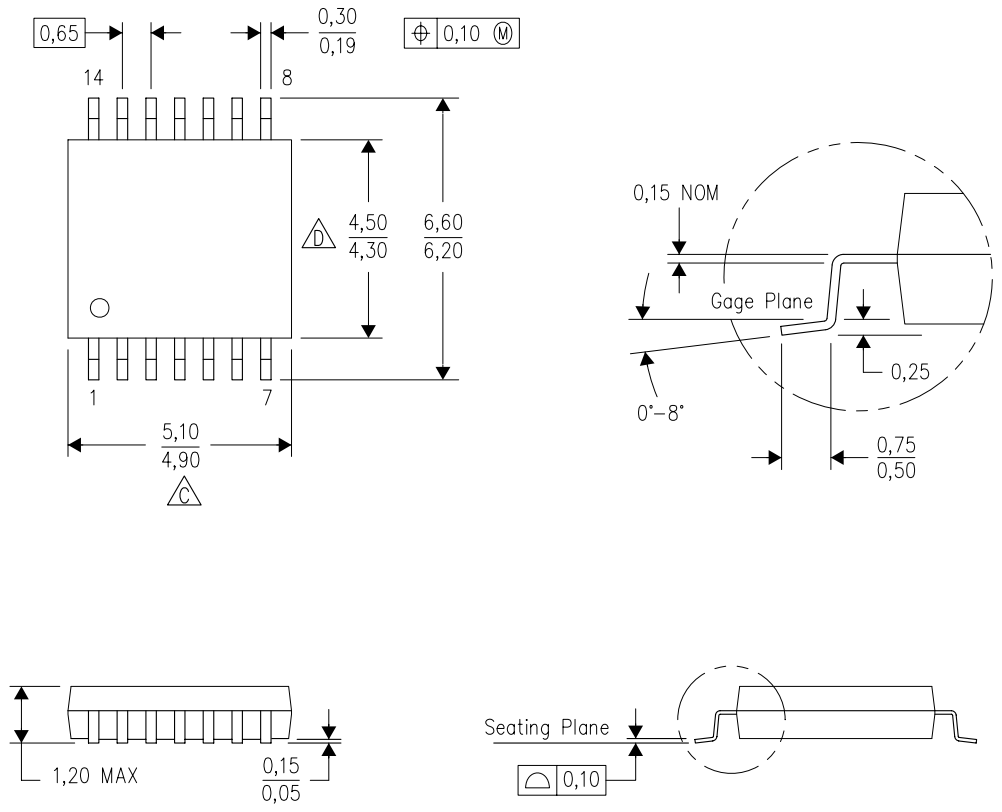
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

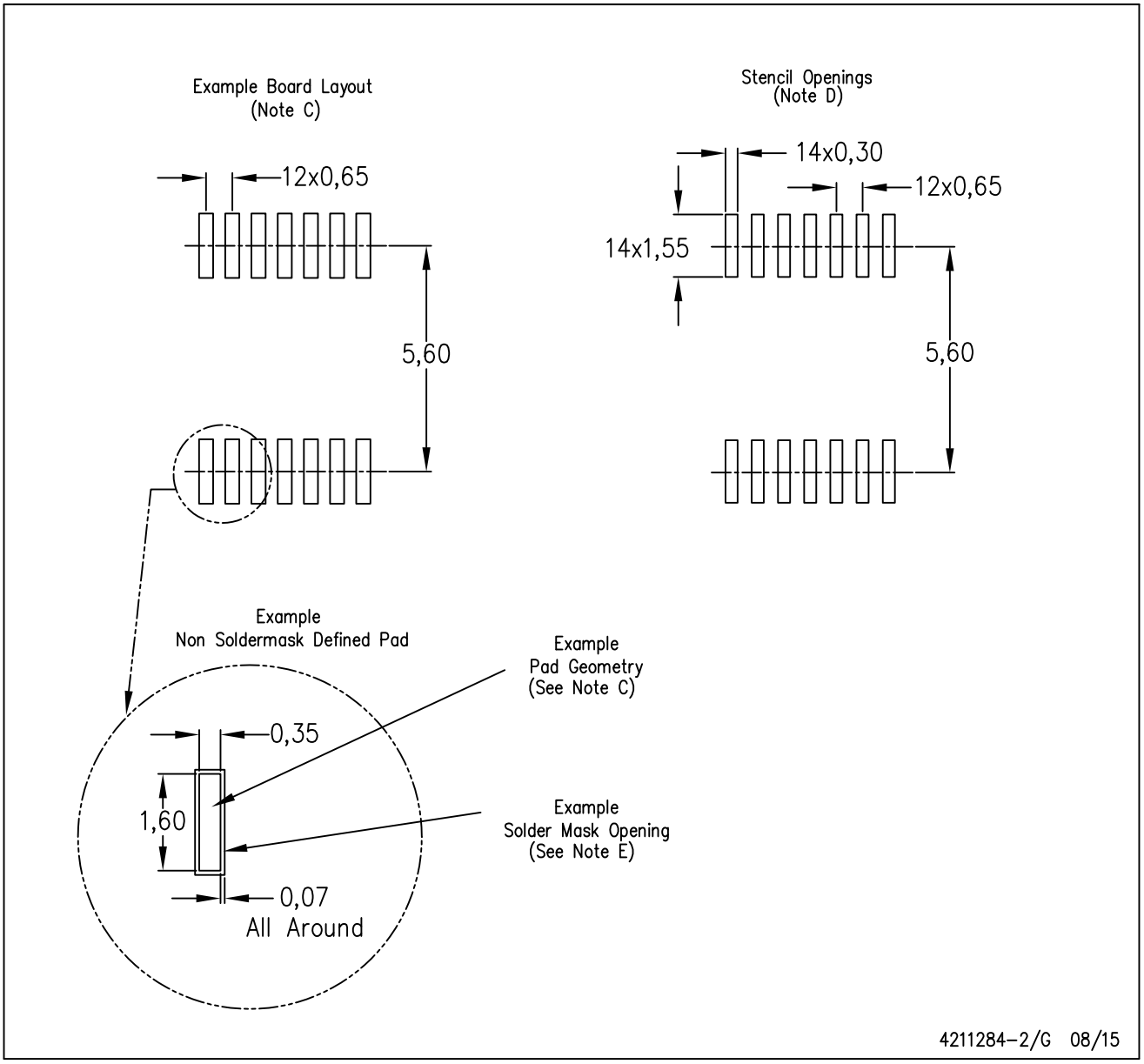
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

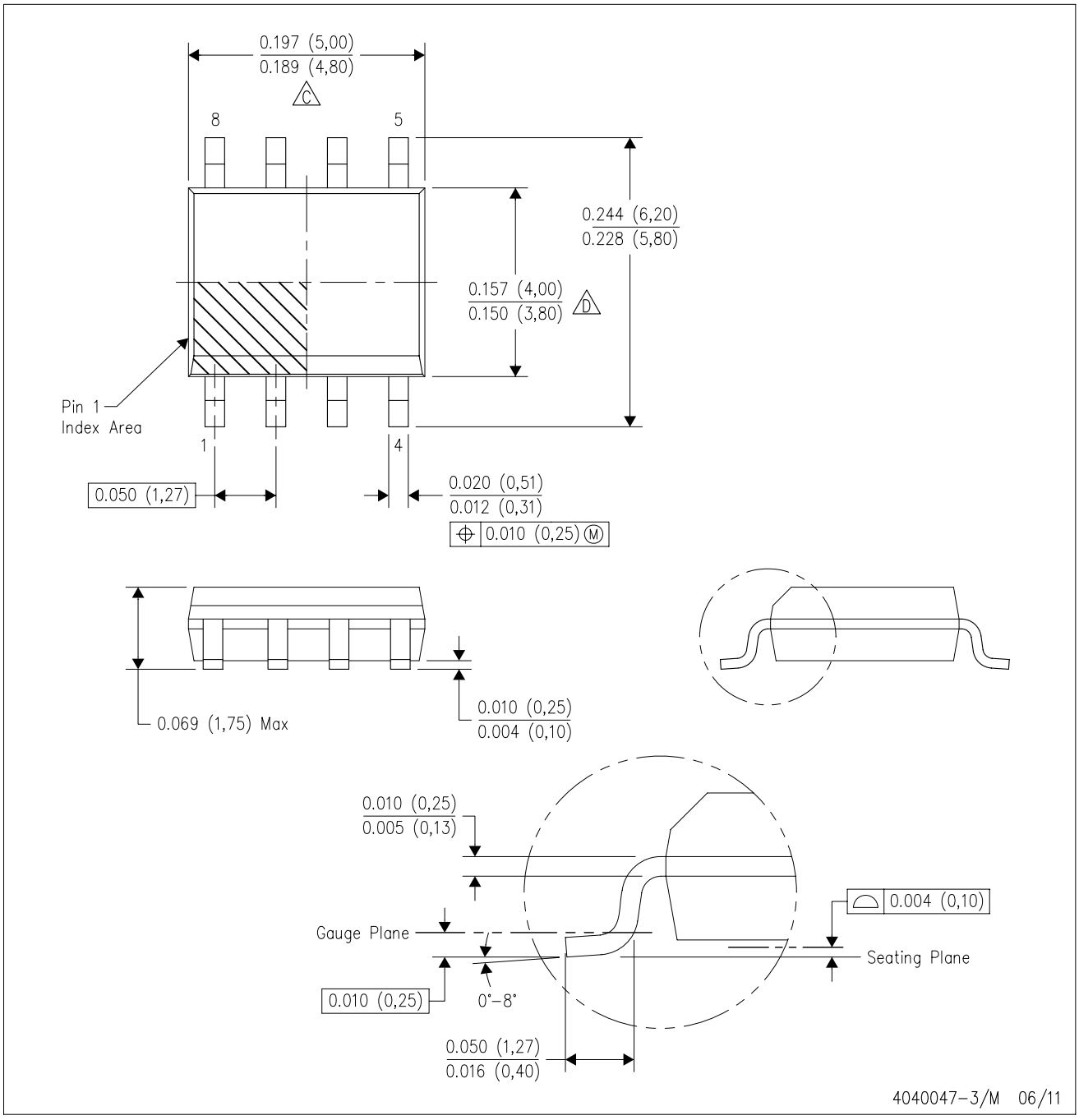
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



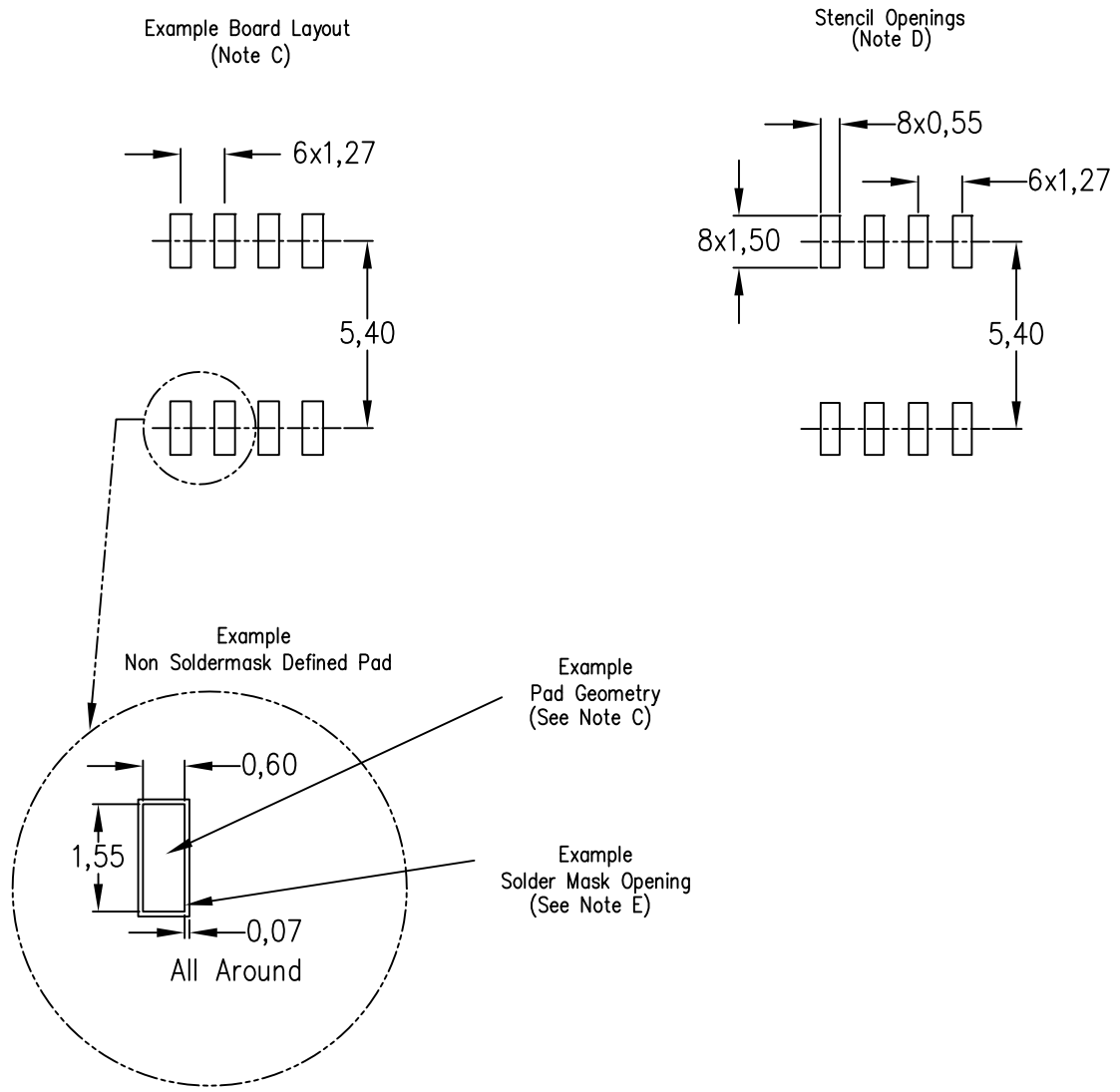
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



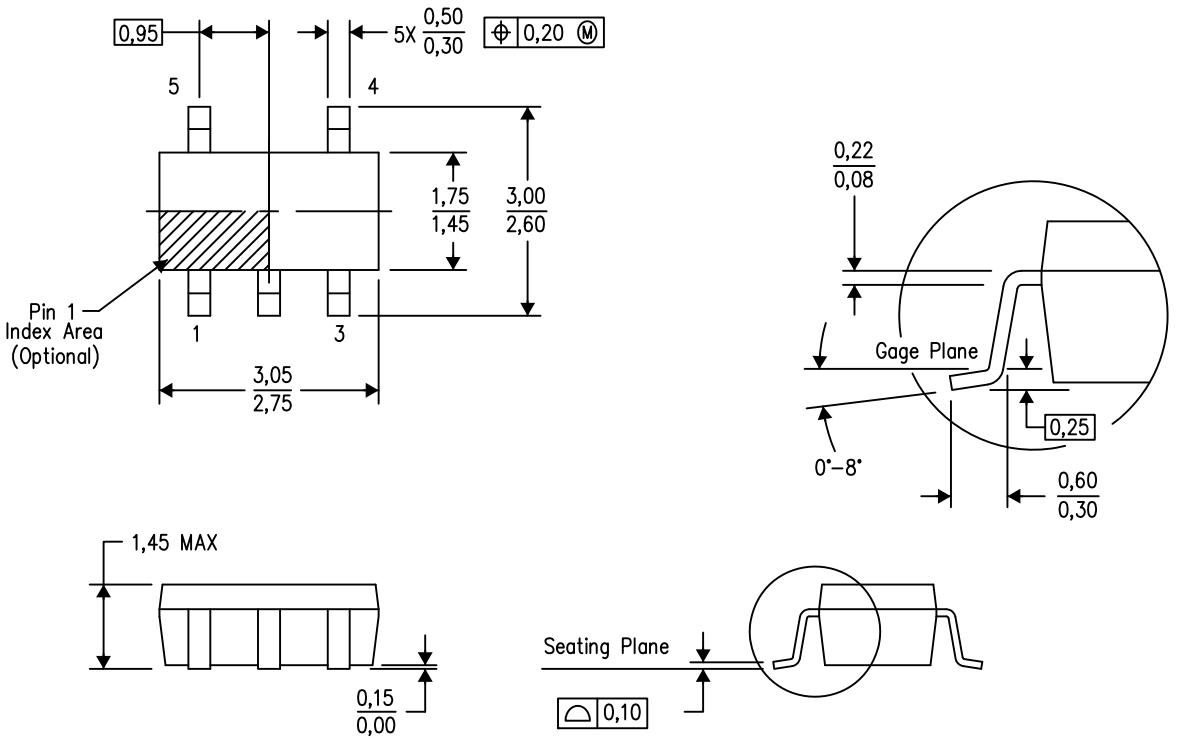
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

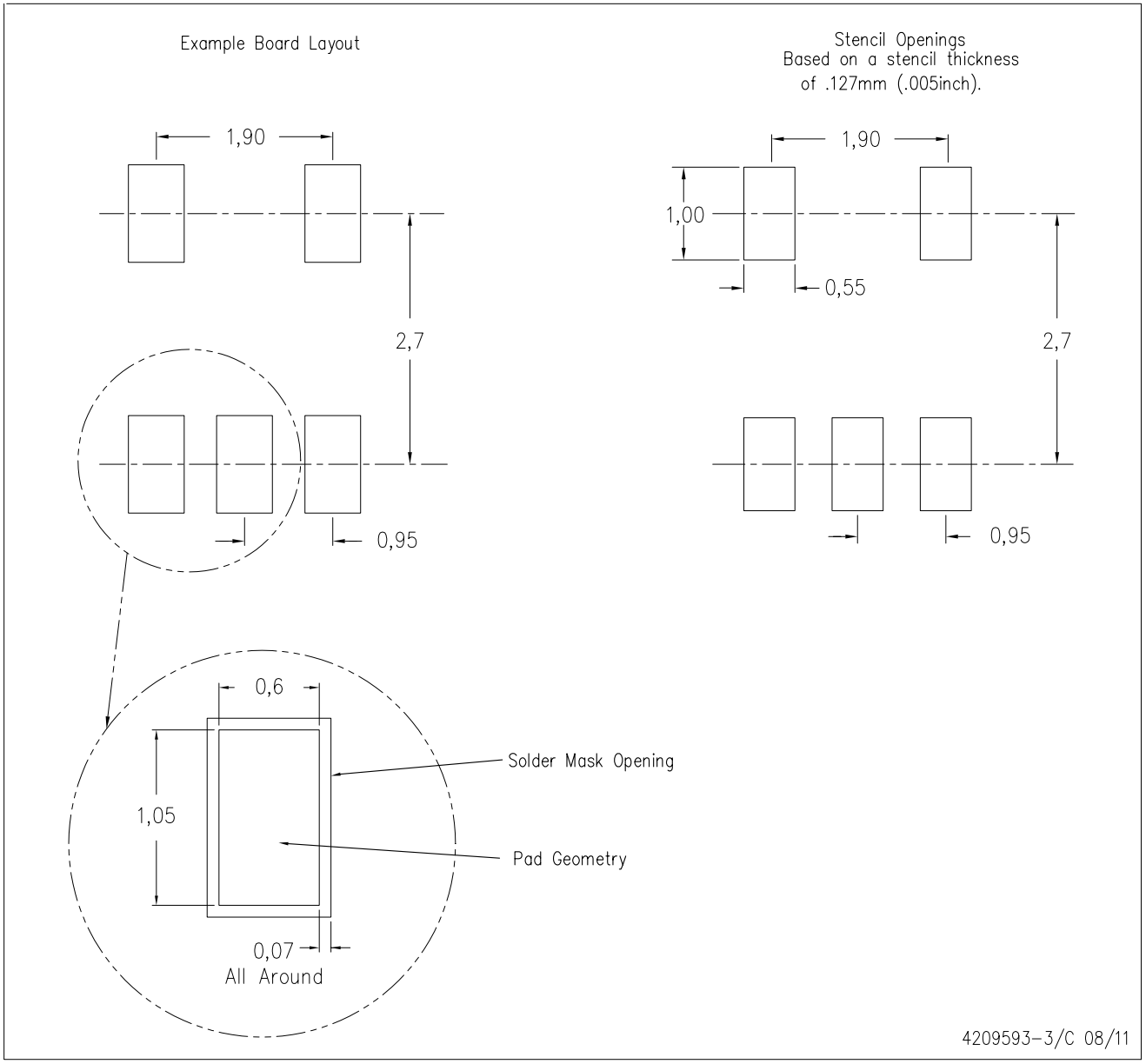
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

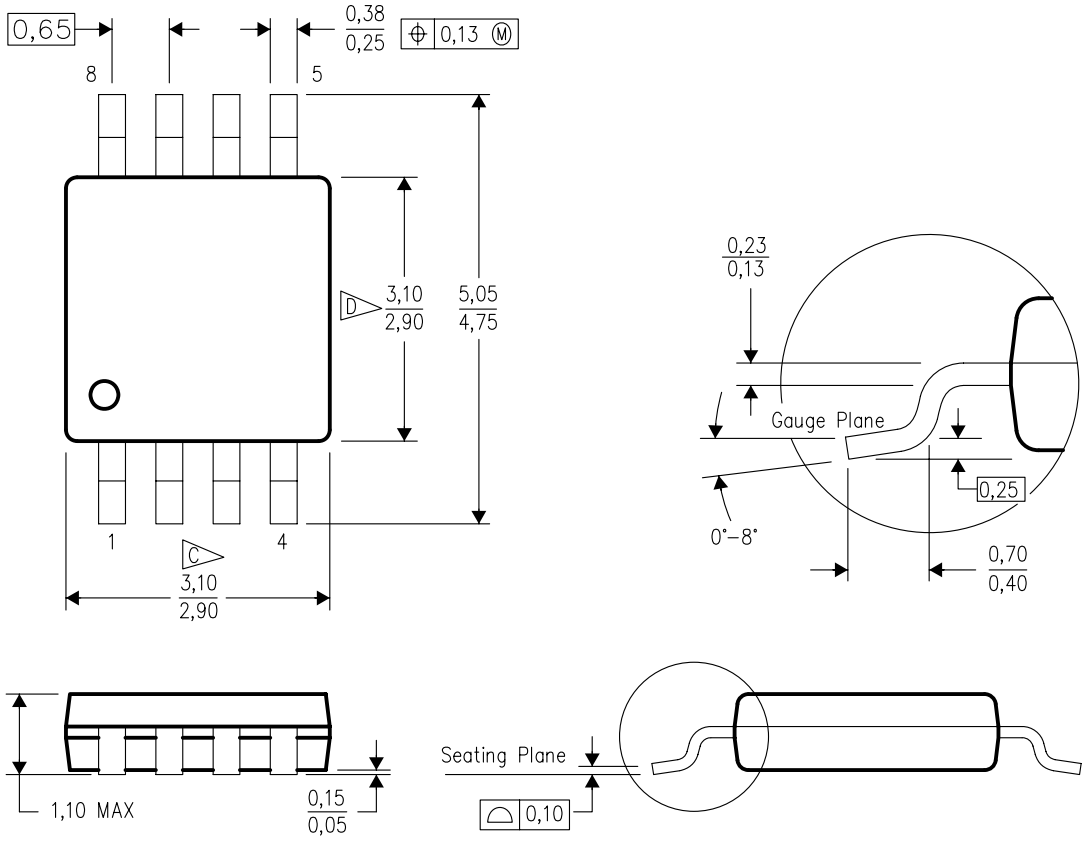
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

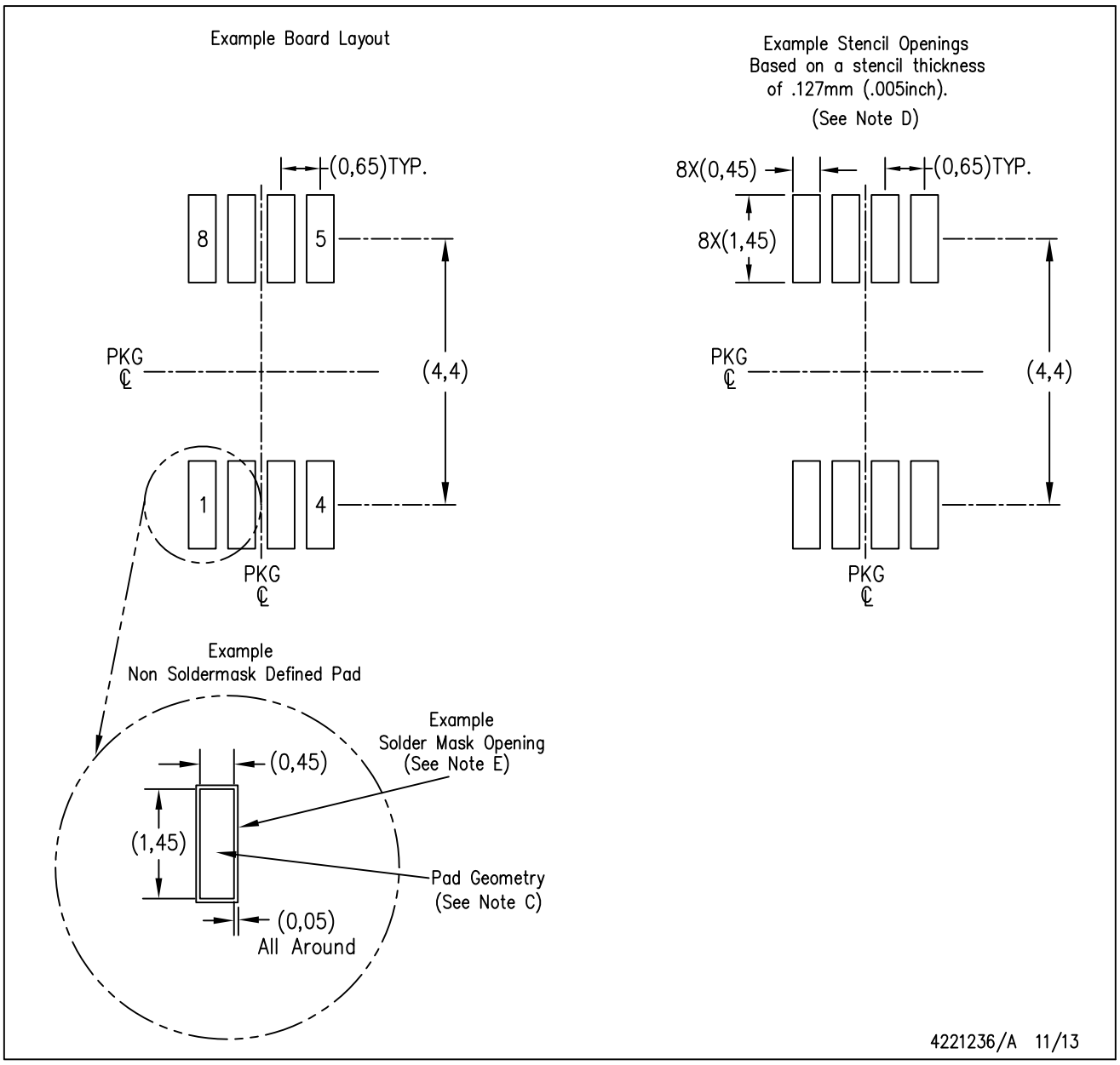
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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