Applications Note: SY5802B

Single Stage Flyback and PFC Controller with Primary Side Control for LED Lighting and Multiple Dimming Mode Option

Preliminary Specification

General Description

The SY5802B is a single stage Flyback and PFC controller targeting at LED Dimming applications. It is a primary side controller without applying any secondary feedback circuit for low cost, and drives the converter in the quasi-resonant mode to achieve higher efficiency. It keeps the converter in constant on time operation to achieve high power factor.

Ordering Information

SY5802 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5802BFAC	SO8	----

Features

- Primary side control eliminates the opto-coupler.
- Compatible with multiple dimming modes.
- Valley turn-on of the primary MOSFET to achieve low switching losses
- 0.3V primary current sense reference voltage leads to a lower sense resistance thus a lower conduction loss.
- Internal high current MOSFET driver: 1A sourcing and 2A sinking
- Low start up current: 15μA typical
- Reliable short LED and Open LED protection
- Power factor >0.90 with single-stage conversion.(Analog dimming only)
- Compact package: SO8

Applications

- LED Dimming

Typical Applications

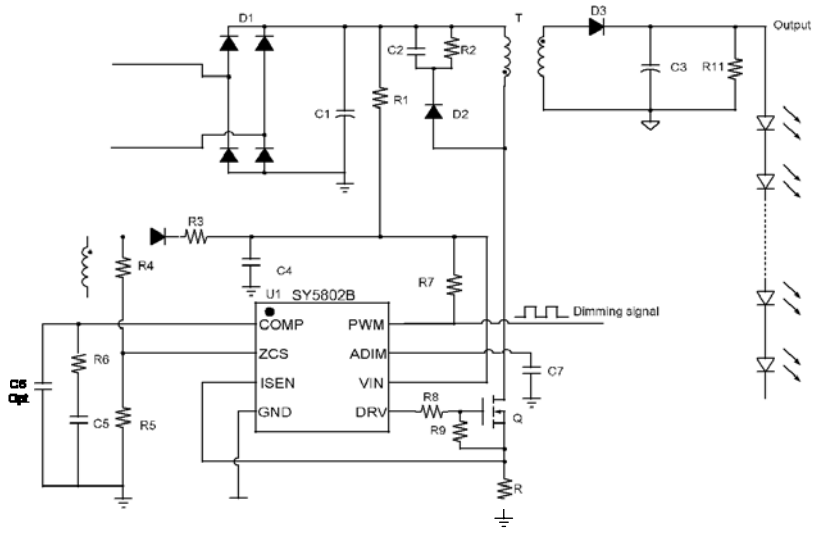


Figure.1a Dimming mode: Analog output with PWM dimming signal

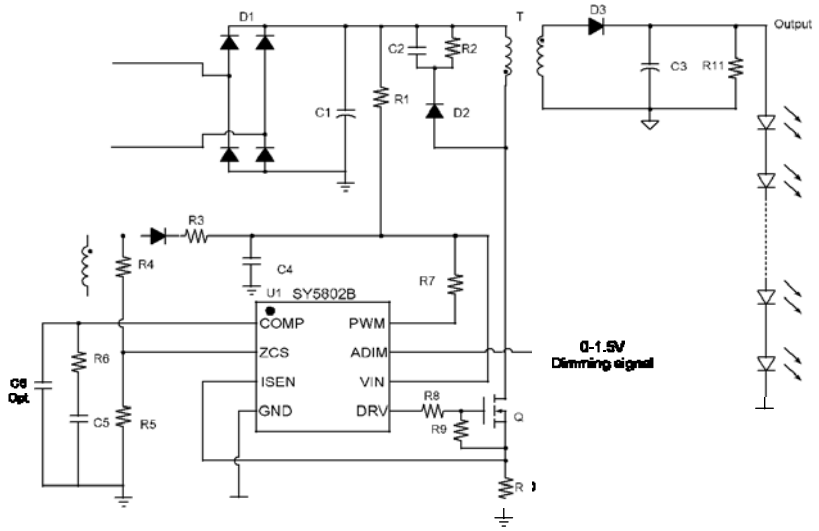


Figure.1b Dimming mode: Analog output with 0-1.5V dimming signal

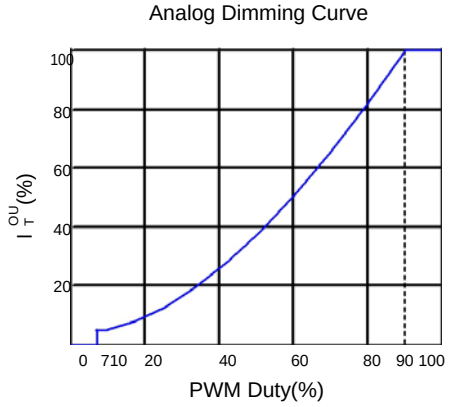


Figure.1c Dimming curve of Analog dimming

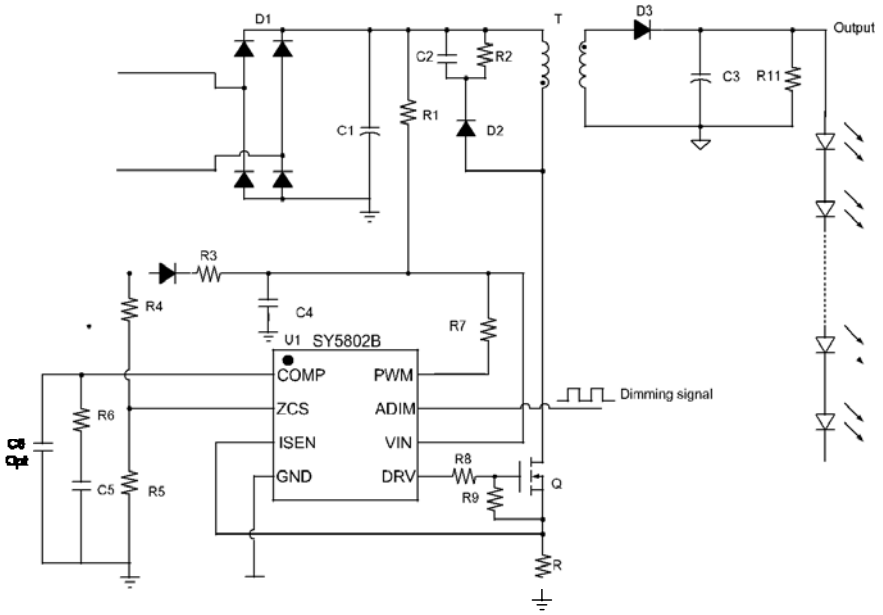


Figure.2a Dimming mode: PWM output with PWM dimming signal

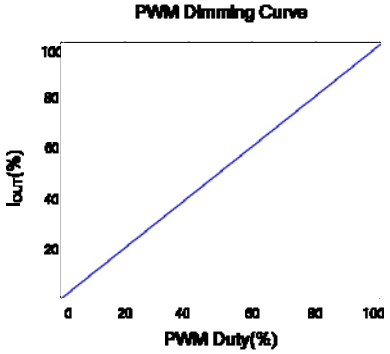
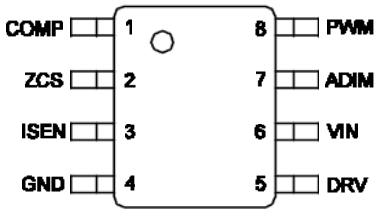


Figure.2b Dimming curve of PWM dimming

Pinout (top view)



(SO8)

Top Mark: AZW *xyz* (device code: AZW, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
COMP	1	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
ZCS	2	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection and line regulation modification function simultaneously. If the voltage on this pin is above $V_{ZCS,OVP}$, the IC would enter over voltage protection mode. Good line regulation can be achieved by adjusting the upper resistor of the divi er.
ISEN	3	Current sense pin. Connect this pin to the source of the primary switch. Connect the sense resistor across the source of the primary switch and the GND pin. (current sense resister R_S : $R_S = k\frac{V_{REF} \times N_{PS}}{I_{OUT}}$, k=0.167)
GND	4	Ground pin
DRV	5	Gate driver pin. Connect this pin to the gate of primary MOSFET.
VIN	6	Power supply pin. This pin also provides output over voltage protection along with ZCS pin.
ADIM	7	Bypass this pin to GND with enough capacitance to hold on internal voltage reference.
PWM	8	PWM dimming input pin, this pin detects the PWM dimming signal

Absolute Maximum Ratings (Note 1)

VIN, DRV	-0.3V~19V
Supply current I_{VIN}	30mA
ADIM, ZCS	- 0.3V~V_{IN}+0.3V
ISEN, COMP, PWM	-0.3~ 3.6V
Power Dissipation, @ T_A = 25°C SO8	1.1W
Package Thermal Resistance (Note 2)	
SO8, θ JA	88°C/W
SO8, θ JC	45°C/W
Junction Temperature Range	40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV	8V~15.4V
Junction Temperature Range	40°C to 125°C

Block Diagram

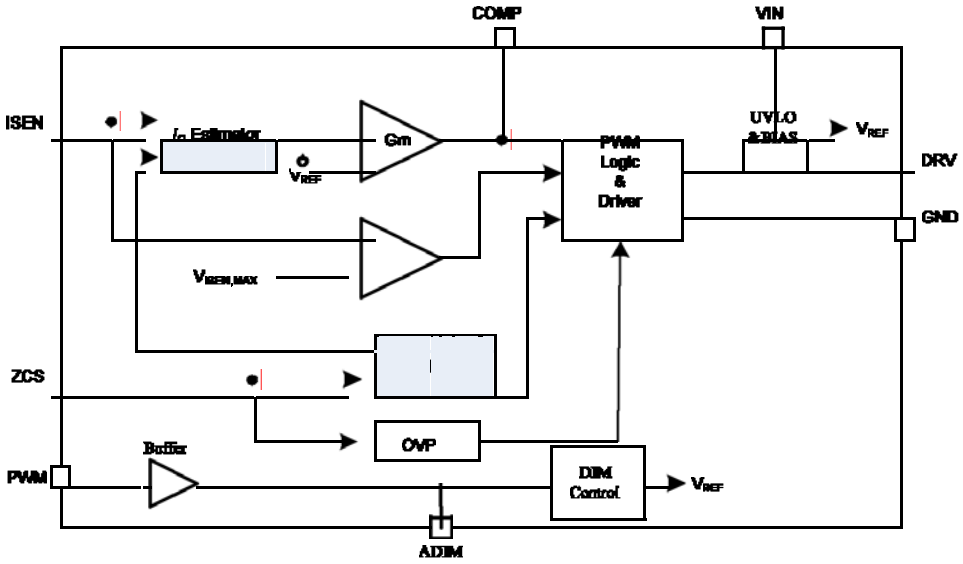


Figure.3 Block Diagram

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input voltage range	V_{VIN}		8		15.4	V
VIN turn-on threshold	$V_{VIN,ON}$				17.6	V
VIN turn-off threshold	$V_{VIN,OFF}$		6.0		7.9	V
VIN OVP voltage	$V_{VIN,OVP}$			$V_{VIN,ON}$+0.85		V
Start up Current	I_{ST}	$V_{VIN} < V_{VIN,OFF}$		15		µA
Operating Current	I_{VIN}	C_L=100pF,f=15kHz		1		mA
Shunt current in OVP mode	$I_{VIN,OVP}$	$V_{VIN} > V_{VIN,OVP}$	1.6	2	2.5	mA
Error Amplifier Section						
Internal reference voltage	V_{REF}		0.294	0.3	0.306	V
Current Sense Section						
Current limit reference voltage	$V_{ISEN,MAX}$			0.4		V
ZCS pin Section						
ZCS pin OVP voltage threshold	$V_{ZCS,OVP}$			1.42		V
Gate Driver Section						
Gate driver voltage	V_{Gate}			V_{VIN}		V
Maximum source current	I_{SOURCE}			1		A
Minimum sink current	I_{SINK}			2		A
Max ON Time	$I_{ON,MAX}$	V_{COMP}=1.5V		24		µs
Min ON Time	$I_{ON,MIN}$			400		ns
Max OFF Time	$I_{OFF,MAX}$			39		µs
Min OFF Time	$I_{OFF,MIN}$			2		µs
Maximum switching frequency	I_{MAX}			90		kHz
ADIM function Section						
ADIM Enable ON	$V_{ADIM,ON}$			0.105		V
Analog dimming range on ADIM	$V_{ADIM,Dimming}$		0.105		1.35	V
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
PWM function Section						
PWM ON current	$I_{PWM,ON}$			20		µA
PWM OFF current	$I_{PWM,OFF}$			10		µA
PWM current Range	I_{PWM}				1	mA

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: f_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

The SY5802B is a single stage Flyback and PFC controller targeting at LED lighting applications with dimming function.

The Device provides primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

SY5802B is compatible with Analog dimming and PWM dimming for different application.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; the start up current of SY5802B is rather small (15μA typically) to reduce the standby power loss further;

the maximum switching frequency is clamped to 120kHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

SY5802B provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY5802B is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND in is charged up by BUS voltage through a start up esistor R_{ST}. Once V_{VIN} rises up to V_{VIN-ON}, the internal bl cks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of transformer could supply enough energy to maintain V_{VIN} above $V_{VIN-OFF}$.

The who e start up procedure is divided into two sections shown in Fig.4. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

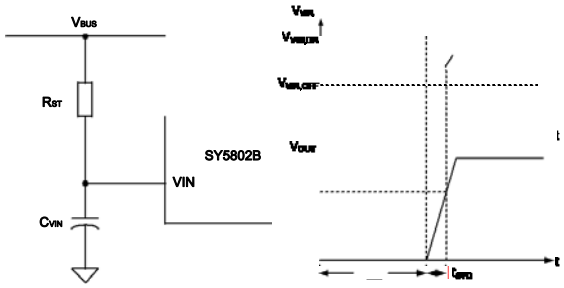


Fig.4 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Internal pre-charge design for quick start up

After V_{VIN} exceeds $V_{VIN,ON}$, V_{ADIM} and V_{COMP} is pre-charged by internal current sources in turn. V_{ADIM} is pre-charged first, and when V_{ADIM} is over the initial voltage $V_{ADIM,IC}$, V_{COMP} begins to be pre-charged. The PWM block won't start to output PWM signals until V_{COMP} is over the initial voltage $V_{COMP,IC}$. $V_{COMP,IC}$ can be programmed by R_{COMP}. Such design is meant to reduce the start up time shown in Fig.5.

The voltage pre-charged V_{COMP_IC} in start-up procedure can be programmed by R_{COMP}

$$V_{COMP\_IC} = 600mV - 300\mu A \times R_{COMP} \quad (3)$$

The voltage pre-charged $V_{ADIM,IC}$ in start-up procedure is fixed internally.

$V_{ADIM,IC} = 750mV$

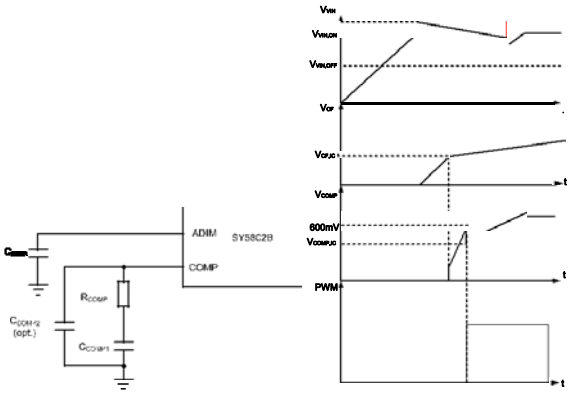


Fig.5 pre-charge scheme in start up

Where $V_{COMP-IC}$ is the pre-charged voltage of COMP pin.

Generally, a big capacitance of C_{COMP} is necessary to achieve high power factor and stabilize the system loop (1μF~2μF recommended).

The voltage pre-charged in start-up procedure can be programmed by R_{COMP}; On the other hand, larger R_{COMP} can provide larger phase margin for the control loop; A small ceramic capacitor is added to suppress high frequency interruption (10pF~100pF is recommended f necessary)

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of the transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN-OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Primary-side constant-current control

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler, which reduces the circuit cost. The switching waveforms are shown in Fig.6.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S} \quad (4)$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of the transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

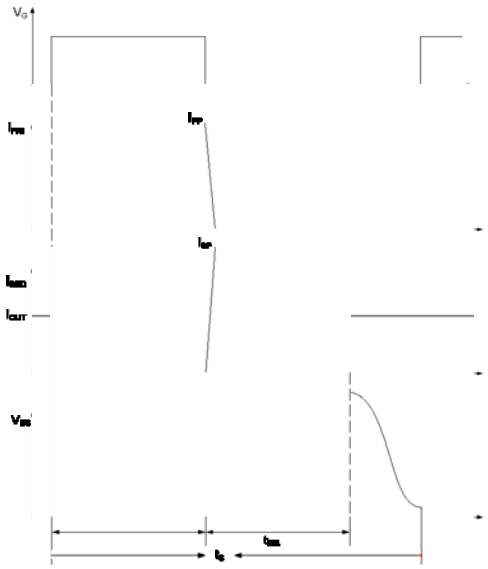


Fig.6 Switching waveforms

$$I_{SP} = N_{PS} \times I_{PP} \quad (5)$$

Where N_{PS} is the turns ratio of primary to secondary of the transformer.

Thus, I_{OUT} can be represented by

$$I_{OUT} = \frac{N_{PS} \times I_{PP}}{2} \times \frac{t_{DIS}}{t_S} \quad (6)$$

The primary peak current I_{PP} and inductor current discharge time t_{DIS} can be detected by Source and ZCS pin, which is shown in Fig.7.These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PP} \times R_S \times \frac{t_{DIS}}{t_S} \times k_1 \quad (7)$$

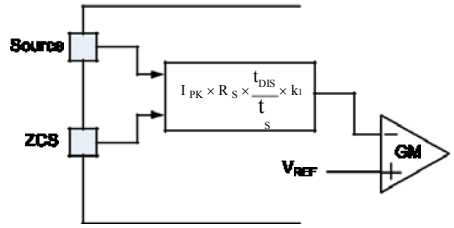


Fig.7 Output current detection diagram

Finally, the output current I_{OUT} can be represented by

$$I_{OUT} = \frac{V_{REF} \times N_{PS}}{R_S \times 2 \times k_1} \quad (8)$$

Where k_1 is the output current weight coefficient; k_2 is the output modification coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT} can be programmed by N_{PS} and R_S.

$$Rs = \frac{V_{REF} \times N_{PS}}{I_{OUT} \times 2 \times k_1} \quad (9)$$

Then

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}, k = \frac{1}{2k_1} \quad (10)$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for the converter.

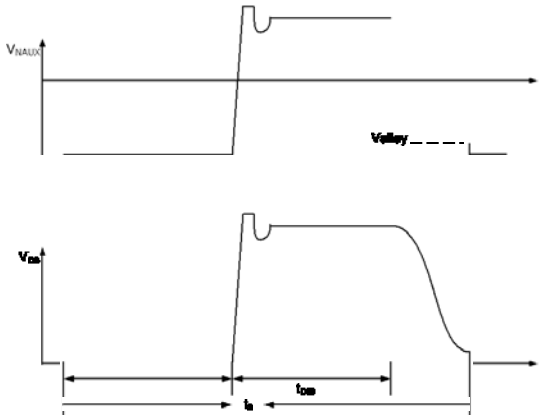


Fig.8 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. ZCS pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

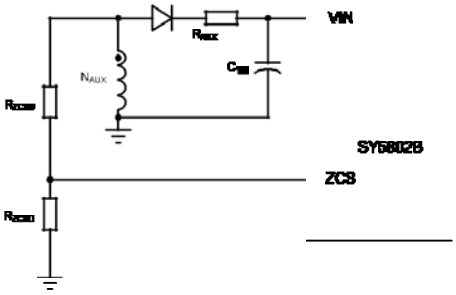


Fig.9 OVP& LP

The output voltage is reflected by the auxiliary winding voltage of the Flyback t ansformer, and both ZCS pin and VIN pin provide over v ltage protection function. When the load is null or large transient happens, the output voltage will xceed the rated value. When V_{VIN} exceeds $V_{VIN,OVP}$ or V_{ZCS} exceeds $V_{ZCS,OVP}$, the over voltage protection is triggered and the IC will discharge V_{VIN} by an int rnal current source $I_{VIN,OVP}$. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{ZCS\_OVP}}{V_{OVP}} = \frac{N_{AUX}}{N_S} \times \frac{R_{ZCSD}}{R_{ZCSU} + R_{ZCSD}} \quad (11)$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}} \geq \frac{N_{AUX}}{N_S} \quad (12)$$

Where V_{OVP} is the output over voltage specification; R_{ZCSU} and R_{ZCSD} compose the resistor divider. The turns ratio of N_S to N_{AUX} and the ratio of R_{ZCSU} to R_{ZCSD} could be induced from equation (11) and (12).

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged

again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed (10Ω typically) shown in Fig.9.

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN-C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to ZCS pin.

$$\Delta V_{ISEN,C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{K_{ZCSU}} \times k_2 \quad (13)$$

Where R_{ZCSU} is the upper resistor of the divider ; k_2 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{ZCSU}, larger compensation is achieved with smaller R_{ZCSU}. Normally, R_{ZCS} ranges from 100kΩ~1MΩ.

Then R_{ZCSD} can be selected by,

$$\frac{\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU} > R_{ZCSD} \quad (14),$$

And,

$$R_{ZCSD} \le \frac{\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU} \quad (15)$$

Where V_{OVP} is the output over voltage protection specification; V_{OUT} is the rated output voltage; R_{ZCSU} is the upper esistor of the divider; N_S and N_{AUX} are the turns of s condary winding and auxiliary winding separately.

Dimming Mode

SY5802B supports two dimming modes: Analog dimming and PWM dimming.

Analog Dimming Mode

In Analog dimming mode, SY5802B is compatible with two dimming signal: PWM dimming signal and 0-1.5V dimming signal, the output current is regulated by the voltage on ADIM pin.

If the dimming signal is PWM signal, it is given to PWM pin. PWM pin detects PWM signal by the current through this pin. When the current is higher than $I_{PWM,ON}$, the dimming signal is sensed as high logic level, and ADIM pin is pulled up to 1.5V by a 300kΩ resistor; when the current is lower than $I_{PWM,OFF}$, the dimming signal is sensed as low logic level, and ADIM pin is pulled down to GND by a 300kΩ resistor. The duty cycle of the dimming signal D_{DIM} is reflected by the voltage on ADIM pin V_{ADIM}.

$$V_{ADIM} = D_{DIM} \times 1.5V$$

When V_{ADIM} is lower than 0.105V (D_{DIM} is 7%), the output current is zero; When V_{ADIM} is from $V_{ADIM,ON}$ to 0.15V (D_{DIM} is from 7% to 10%), the output current is 10% of r ted output current; When V_{ADIM} is higher than 1.35V (D_{DIM} is over 90%), the output current is 100% of rat d output current; When V_{ADIM} is in the range from 0.15V to 1.35V (D_{DIM} is from 10% to 90%), I_{OUT} increases with D_{DIM} linearly from 10% to 100% of rated output current.

The dimming curve between output current I_{OUT}, V_{ADIM} and duty cycle of dimming signal is shown as below.

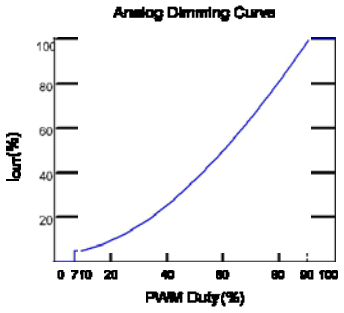


Fig.10 Dimming curve of analog dimming

A capacitor C_{ADIM} need be connected across ADIM and GND pin to obtain a smooth voltage waveform of the dimming signal duty cycle. C_{ADIM} is selected by

$$C_{ADIM} = \frac{1.25 \times 10^{-5}}{f_{DIM}} F \times Hz \quad (16)$$

Where f_{DIM} is the frequency of PWM dimming signal.

If the dimming signal is analog voltage, the dimming signal is given to ADIM pin directly. PWM pin should be pulled up to VIN by a resistor R_{PWM} or pulled down to GND.

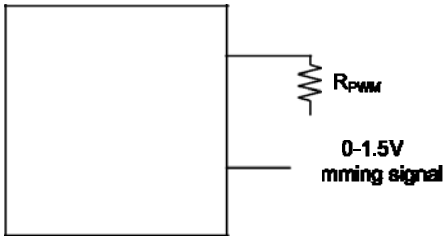


Fig.11 Connection of Analog dimming with 0-1.5V dimming signal

PWM Dimming Mode

In PWM dimming mode, the output current is chopped by the dimming signal directly, the dimming function is shown as below.

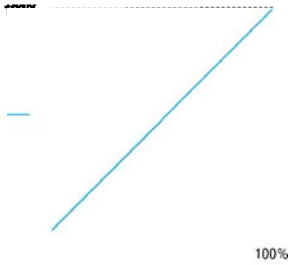


Fig.12 PWM dimming curve

In PWM dimming mode, the dimming sig al is given to ADIM pin. The logic voltage level of the Dimming signal is limited by

$$V_{VIN} > V_{DimH} > 1.35V \quad (17)$$

$$V_{DimL} < V_{ADIM,ON} \quad (18)$$

Where V_{DimH} is logic high level of the Dimming signal, V_{DimL} is logic low level of the Dimming signal.

And a resistor $R_{ADIM,up}$ need be connected across ADIM and VIN pin (1MΩ recommeded).

Power Device Design

Power Device Design for Analog Dimming

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (19)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (20)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (21)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (22)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (23)$$

$$I_{D\_AVG} = I_{OUT} \quad (24)$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (25)$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current

falling time t_2 and quasi-resonant time t_3 shown in Fig.13.

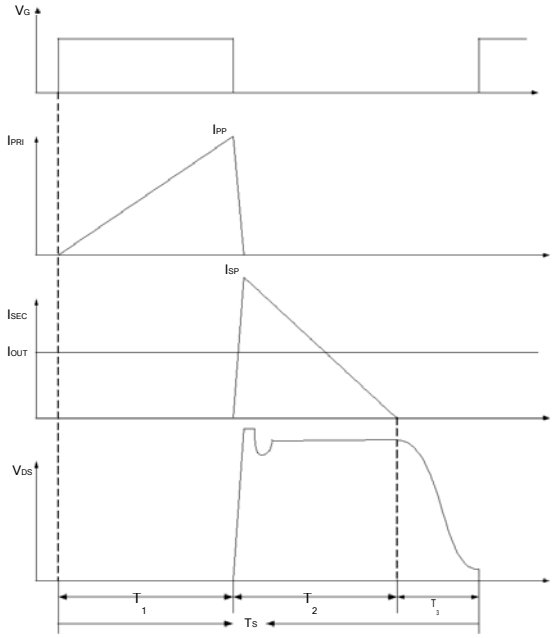


Fig.13 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happe s at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; Meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (26)$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}} \quad (27)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}} \quad (28)$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \quad (29)$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (30)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta} \quad (31)$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}} \quad (32)$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \quad (33)$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} \quad (34)$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (35)$$

$$t_2' = t_S' - t_1' - t_3 \quad (36)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} \quad (37)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P-PK-MAX}$
Primary maximum RMS current	$I_{P-RMS-MAX}$
Secondary maximum RMS current	$I_{S-RMS-MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (38)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (39)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (40)$$

Where V_{VIN} is the working voltage of VIN pin (10V~11V is recommended).

(f) Select an appropriate wire diameter

With $I_{P-RMS-MAX}$ and $I_{S-RMS-MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT} = \frac{\sqrt{2\left(\frac{I_{OUT}}{\Delta I_{OUT}}\right)^2 - 1}}{4\pi f_{AC} R_{LED}} \quad (41)$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (42)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; V_{D-F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (43)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (44)$$

Power Device Design for PWM Dimming

Input BUS Capacitor (C_{BUS})

The input BUS capacitor is selected by

$$C_{BUS} = P_{IN} \times \frac{\arcsin(1-\Delta V_{IN}) + \frac{\pi}{2}}{\pi \times f_{IN} \times \left(\sqrt{2} \times V_{AC,MIN}\right)^2 \times \left(1 - (1-\Delta V_{IN})^2\right)} \quad (45)$$

Where P_{IN} is the input power, $V_{AC,MIN}$ is the minimum input AC voltage, f_{in} is the input AC frequency, ΔV_{IN} is the input voltage ripple ratio.

As general engineering application, the input BUS Capacitor can also be selected simply by

$$C_{BUS} = P_{IN} \times (2\sim3)\mu F/W \quad (46)$$

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (47)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (48)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (49)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (50)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (51)$$

$$I_{D\_AVG} = I_{OUT} \quad (52)$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (53)$$

Where $V_{MOS,(BR)DS}$ is the b eakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.14.

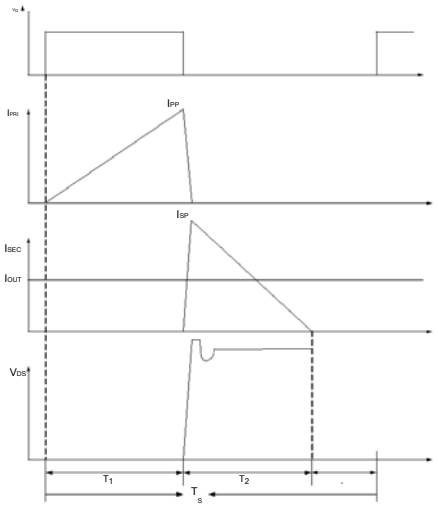


Fig.14 switching waveforms

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (54)$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}} \quad (55)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (56)$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \quad (57)$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (58)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX}=\frac{P_{OUT}\times\left[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}\right]}{L_M\times\eta}+\sqrt{P_{OUT}^2\times\left[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}\right]^2+L_M\times\eta\times P_{OUT}\times t_s}{L_M\times\eta}} \quad (59)$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_s'=\frac{\eta\times L_M\times I_{P\_PK\_MAX}^2}{2P_{OUT}} \quad (60)$$

$$t_1'=\frac{L_M\times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \quad (61)$$

$$I_{P\_RMS\_MAX}\approx\sqrt{\frac{t_1'}{3t_s'}}\times I_{P\_PK\_MAX} \quad (62)$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (63)$$

$$t_2'=t_s'-t_1'-t_3 \quad (64)$$

$$I_{S\_RMS\_MAX}\approx\sqrt{\frac{t_2'}{3t_s'}}\times I_{S\_PK\_MAX} \quad (65)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P=\frac{L_M\times I_{P\_PK\_MAX}}{\Delta B\times A_e} \quad (66)$$

(d) Compute secondary turn N_S

$$N_S=\frac{N_P}{N_{PS}} \quad (67)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX}=N_S\times\frac{V_{VIN}}{V_{OUT}} \quad (68)$$

Where V_{VIN} is the working voltage of VIN pin (10V~11V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Generally , the output voltage ripple is up to the ESR of the output capacitor C_{OUT}.
Preset the output current ripple, C_{OUT} is induced by

$$R_{Cout,ESR}=\frac{\Delta V_{OUT}}{I_{S\_PK\_MAX}} \quad (69)$$

Where $R_{Cout,ESR}$ is the ESR of C_{OUT}.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT} \quad (70)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the

inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}}(71)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

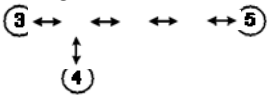
$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}\ f_S\ \Delta V_{C\_RCD}}(72)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor and GND pin
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace except GND pin
Ground ⑤: primary ground node of Y capacitor.
Ground ⑥: ground node of current sample resistor.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(f) Loop of 'Source pin – current sample resistor – GND pin' .should be kept as small as possible.

(f) The resistor divider is recommended to be put beside the IC.

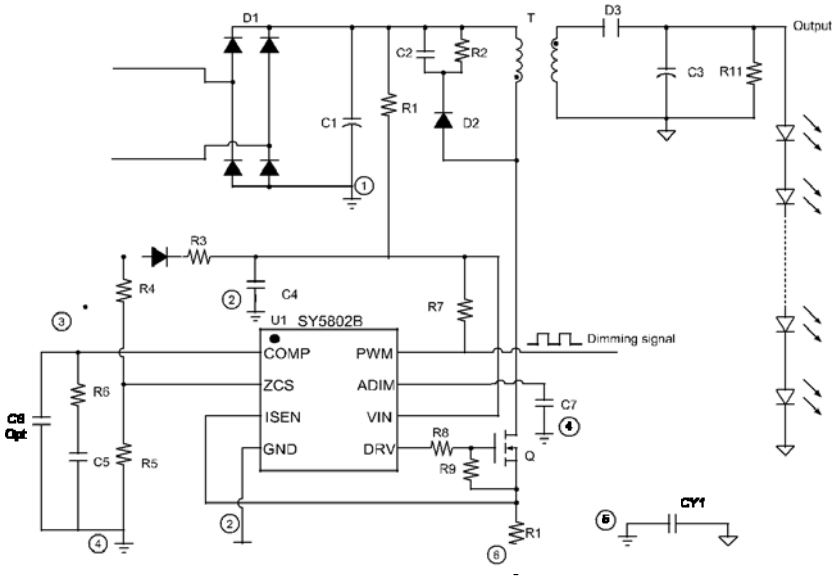


Fig.15 Ground connection recommended

Design Example

A design example of typical application is shown below step by step.

1. Analog dimming design Example

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	38V
I_{OUT}	320mA	η	87%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	90V	V_{AC-MAX}	264V
ΔV_S	50V	$V_{MOS-(BR)DS}$	600V
P_{OUT}	12W	$V_{D,F}$	1V
C_{Drain}	100pF	f_{S-MIN}	75kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 50V}{38V + 1V}$$

$$= 2.99$$

N_{PS} is set to

$$N_{PS} = 2.67$$

(b)$f_{S,MIN}$ is preset

$$f_{S\_MIN} = 75kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 13.3\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

$$= \frac{13.3\mu s \times 2.67 \times (38V + 1V)}{\sqrt{2} \times 90V + 2.67 \times (38V + 1V)}$$

$$= 6\mu s$$

(d) Compute the inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$
$$= \frac{90V^2 \times 6\mu s^2 \times 0.87}{2 \times 12W \times 13.3\mu s}$$
$$= 780\mu H$$

Set

$$L_M = 750\mu H$$

(e) Compute the quasi-resonant time t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$
$$= \pi \times \sqrt{750\mu H \times 100pF}$$
$$= 860ns$$

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta}$$
$$+ \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$
$$= 1.038A$$

Adjust switching period t_S and ON time t_1 to t'_S and t'_1.

$$t'_S = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$
$$= \frac{0.87 \times 750\mu H \times 1.038A^2}{4 \times 12W}$$
$$= 14.45\mu s$$

$$t'_1 = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$
$$= \frac{750\mu H \times 1.038A}{\sqrt{2} \times 90V}$$
$$= 6.12\mu s$$

Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t'_1}{6t'_S}} \times I_{P\_PK\_MAX} = \sqrt{\frac{6.12\mu s}{6 \times 14.45\mu s}} \times 1.038A = 0.289A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.67 \times 1.038A = 2.77A$$

$t'_2 = t'_S - t'_1 - t'_3 = 14.45\mu s - 6.12\mu s - 0.86\mu s = 7.47\mu s$

$$I_{S,RMS,MAX} \approx \sqrt{\frac{t'_2}{6t'_S}} \times I_{S\_PK\_MAX} = \sqrt{\frac{7.47\mu s}{6 \times 14.45\mu s}} \times 2.77A = 0.81A$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{AC-MAX}	264V	N_{PS}	2.67
V_{OUT}	36V	V_{D-F}	1V
V_S	50V	η	87%

(a) Compute the voltage and the current stress of MOSFET:

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$
$$= \sqrt{2} \times 264V + 2.67 \times (38V + 1V) + 50V$$
$$= 527V$$

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 1.038A$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.289A$$

(b) Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$
$$= \frac{\sqrt{2} \times 264V}{2.67} + 38V$$
$$= 178V$$

$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.67 \times 1.038A = 2.77A$

$I_{D\_AVG} = I_{OUT} = 0.32A$

#4. Select the output capacitor C_{OUT}

Refer to Power Device Design

Conditions			
I_{OUT}	320mA	ΔI_{OUT}	$0.3I_{OUT}$
f_{AC}	50Hz	R_{LED}	12× 1.6Ω

The output capacitor is

$$C_{OUT} = \frac{\sqrt{\left(\frac{2I_{OUT}}{\Delta I_{OUT}}\right)^2 - 1}}{4\pi f_{AC} R_{LED}}$$

$$= \frac{\sqrt{\left(\frac{2 \times 032A}{0.3 \times 0.32A}\right)^2 - 1}}{4\pi \times 50Hz \times 12 \times 1.6\Omega}$$

$$= 546\mu F$$

#5. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	38V	ΔV_S	50V
N_{PS}	2.67	L_K/L_M	1%
P_{OUT}	12W		

The power loss of the snubber is

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

$$= \frac{2.67 \times (38V + 1V) + 50V}{50V} \times 0.01 \times 12W$$

$$= 0.37W$$

The resistor of the snubber is

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

$$= \frac{(2.67 \times (38V + 1V) + 50V)^2}{0.37W}$$

$$= 64k\Omega$$

The capacitor of the snubber is

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}}$$

$$= \frac{2.67 \times (38V + 1V) + 50V}{64k\Omega \times 100kHz \times 25V}$$

$$= 1nF$$

#6. Set VIN pin
Refer to **Start up**

Condit ons			
$V_{BUS-MIN}$	90V × 1.414	$V_{BUS-MAX}$	264V× 1.414
I_{ST}	15μA (typical)	V_{IN-ON}	16V (typical)
$I_{VIN-OVP}$	2mA (typical)	t_{ST}	500ms (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{90V \times 1.414}{15\mu A} = 8.48M\Omega ,$$

$$R_{ST} > \frac{V_{BUS}}{I_{VIN\_OVP}} = \frac{264V \times 1.414}{2mA} = 186k\Omega$$

Set R_{ST}

$R_{ST} = 250k\Omega \times 3 = 750k\Omega$

(b) Design C_{VIN}

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

$$= \frac{(\frac{90V \times 1.414}{750k\Omega} - 15\mu A) \times 500ms}{16V}$$

$= 4.83\mu F$

Set C_{VIN}

$C_{VIN} = 20\mu F$

#7 Set COMP pin

Refer to **Internal pre-charge design for quick start up**

Parameters designed			
R_{COMP}	500Ω	$V_{COMP,IC}$	450mV
C_{COMP1}	2μF	C_{COMP2}	100pF

#8 Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k	0.167	N_{PS}	2.67
V_{REF}	0.3V	I_{OUT}	0.32A

The current sense resistor is

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}$$

$$= \frac{0.167 \times 0.3V \times 2.67}{0.32A}$$

$= 0.4\Omega$

#9 set ZCS pin

Refer to **Line regulation modification** and **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First identify R_{ZCSU} need for line regulation.

Known conditions at this step			
R_2	68		
Parameters Designed			
R_{ZCSU}	100kΩ		

Then compute R_{ZCSD}

Conditions			
V_{ZCS_OVP}	1.42V	V_{OVP}	48V
V_{OUT}	38V		
Parameters designed			
R_{ZCSU}	100kΩ		
N_S	21	N_{AUX}	5

$$R_{ZCSD} < \frac{\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU}$$

$$= \frac{\frac{1.42V}{38V} \times \frac{21}{6}}{1-\frac{1.42V}{38V} \times \frac{21}{6}} \times 100k\Omega$$

$$= 18.62k\Omega$$

$$R_{ZCSD} \geq \frac{\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU}$$

$$= \frac{\frac{1.42V}{48V} \times \frac{21}{5}}{1-\frac{1.42V}{48V} \times \frac{21}{5}} \times 100k\Omega$$

$$=14.19k\Omega$$

R_{ZCSD} is set to

R_{ZCSD} =15kΩ

#10 set ADIM and PWM pin

Refer to **Analog Dimming Mode Design**

Conditions			
$V_{VIN,OFF}$	6V	$I_{PWM,ON}$	20μA
$I_{PWM,OFF}$	10μA	f_{Dim}	100Hz
Parameters designed			
$V_{Dim,high}$	10V		

$$R_{PWM,limit} < \frac{V_{Dim,high}}{I_{PWM,ON}} = \frac{10V}{20\mu A} = 500k\Omega$$

$R_{PWM,limit}$ is set to

$R_{PWM,limit}$=50kΩ

$$R_{PWM,up} < \frac{V_{VIN,OFF}}{I_{PWM,ON}} = \frac{6V}{20\mu A} = 300k\Omega$$

So $R_{PWM,up}$ is set to

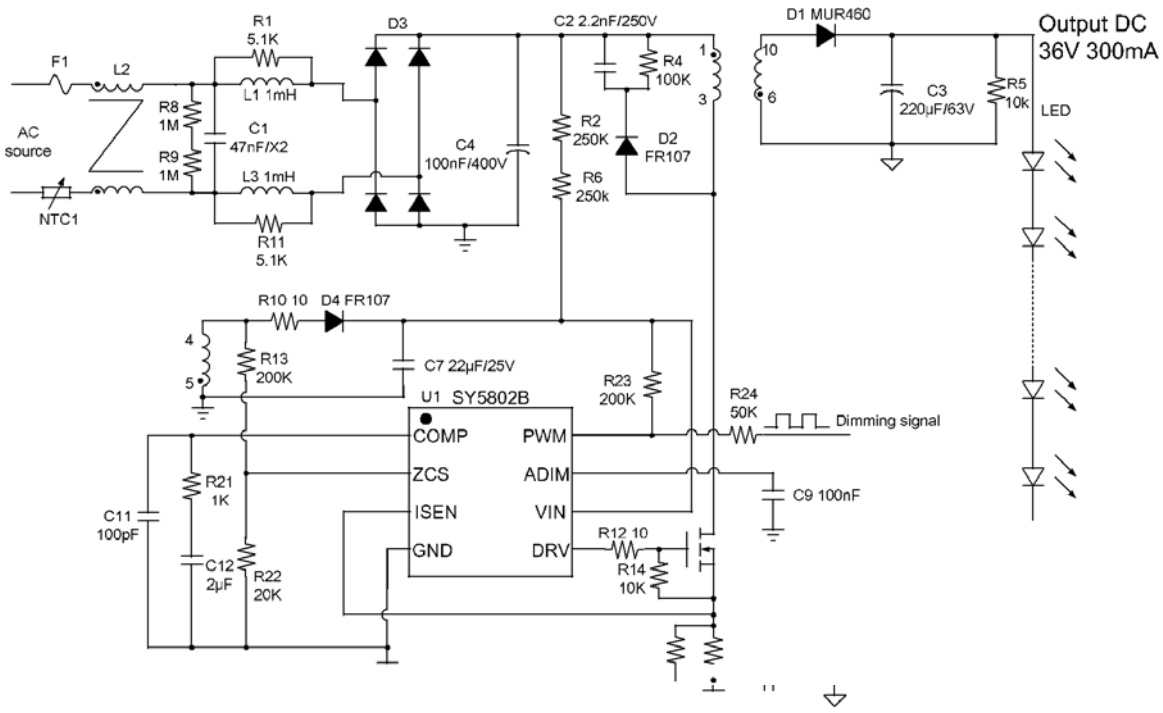
$R_{PWM,up}=200k\Omega$

$$C_{ADIM} = \frac{1.25 \times 10^{-5}\ F \times Hz}{f_{PWM}} = \frac{1.25 \times 10^{-5}\ F \times Hz}{f_{PWM}} = 125nF$$

Hence C_{ADIM} is set to

$C_{ADIM}=100nF$

#11 final result



2. PWM dimming design Example

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	36V
I_{OUT}	300mA	η	85%
ΔV_{in}	0.18		

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	90V	V_{AC-MAX}	264V
ΔV_S	50V	$V_{MOS-(BR)DS}$	600V
I_{OUT}	10.8W	$V_{D,F}$	1V
C_{Drain}	100pF	f_{S-MIN}	50kHz
$V_{DC,MIN}$	104V		

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 50V}{36V+1V}$$

$$=2.99$$

N_{PS} is set to

$N_{PS}=2$

(b)$f_{S,MIN}$ is preset

$f_{S\_MIN}=50kHz$

(c) Compute the switching pe iod t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 20\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT}+V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT}+V_{D\_F})}$$

$$= \frac{20\mu s \times 2 \times (36V+1V)}{\sqrt{2} \times 90V + 2 \times (36V+1V)}$$

$$=9\mu s$$

(d) Compute the inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$

$$= \frac{90V^2 \times 9\mu s^2 \times 0.85}{2 \times 10.8W \times 20\mu s}$$

$$=1.3mH$$

Set

$$L_M = 1.2mH$$

(e) Compute the quasi-resonant time t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$

$$= \pi \times \sqrt{1.2mH \times 100pF}$$

$$=1.09us$$

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$

$$I_{P\_PK\_MAX} = \frac{P_{OUT} \times [\frac{L_M}{V_{DC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{P_{OUT}^2 \times [\frac{L_M}{V_{DC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

$$=0.624A$$

Adjust switching period t_S and ON time t_1 to t'_S and t'_1.

$$t'_S = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{2P_{OUT}}$$

$$= \frac{0.85 \times 1.2mH \times 0.624A^2}{2 \times 10.8W}$$

$$=18.38\mu s$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN} \times (1 - \Delta Vin)}$$

$$= \frac{1.2mH \times 0.624A}{104V}$$

$$=7.19\mu s$$

Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{3t'_S}} \times I_{P\_PK\_MAX} = \sqrt{\frac{7.19\mu s}{3 \times 18.38\mu s}} \times 0.624A = 0.225A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 0.624A = 1.248A$$

$t'_2 = t'_S - t'_1 - t_3 = 18.38\mu s - 7.19\mu s - 1.088\mu s = 10.12\mu s$

$$I_{S,RMS,MAX} \approx \sqrt{\frac{t'_2}{3t'_S}} \times I_{S\_PK\_MAX} = \sqrt{\frac{10.12\mu s}{3 \times 18.38\mu s}} \times 1.248A = 0.534A$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{AC-MAX}	264V	N_{PS}	2
V_{OUT}	36V	V_{D-F}	1V
V_S	50V	η	85%

(a) Compute the voltage and the current stress of MOSFET:

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$
$$= \sqrt{2} \times 264V + 2 \times (36V + 1V) + 50V$$
$$= 497V$$

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 0.624A$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.224A$$

(b) Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$
$$= \frac{\sqrt{2} \times 264V}{2} + 36V$$
$$= 223V$$

$$I_{D\_PK\_MAX} = I_{S\_PK\_MAX} = 1.248A$$

$$I_{D\_AVG} = I_{OUT} = 0.3A$$

#4. Select the output capacitor C_{OUT}

Refer to Power Device Design

Conditions			
ΔV_{OUT}	360mV		

The output capacitor is

$$R_{Cout,ESR} = \frac{\Delta V_{OUT}}{I_{S\_PK\_MAX}} = \frac{50mV}{1.284A} = 280m\Omega$$

#5. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	36V	ΔV_S	50V
N_{PS}	2	L_K/L_M	1%
P_{OUT}	10.8W		

The power loss of the snubber is

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

$$= \frac{2 \times (36V+1V)+50V}{50V} \times 0.01 \times 10.8W$$

$$= 0.27W$$

The resistor of the snubber is

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

$$= \frac{(2 \times (36V+1V)+50V)^2}{0.27W}$$

$$= 60k\Omega$$

The capacitor of the snubber is

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}}$$

$$= \frac{2 \times (36V+1V)+50V}{60k\Omega \times 100kHz \times 25V}$$

$$= 830pF$$

#6. Set VIN pin

Refer to Start up

Conditions			
$V_{BUS-MIN}$	104V	$V_{BUS-MAX}$	264V× 1.414
I_{ST}	15μA (typical)	V_{IN-ON}	16V (typical)
$I_{VIN-OVP}$	2mA (typical)	t_{ST}	500ms (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{90V \times 1.414}{15\mu A} = 8.48M\Omega,$$

$$R_{ST} > \frac{V_{BUS}}{I_{VIN-OVP}} = \frac{264V \times 1.414}{2mA} = 186k\Omega$$

Set R_{ST}

$$R_{ST} = 250k\Omega \times 3 = 750k\Omega$$

(b) Design C_{VIN}

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

$$= \frac{(\frac{104V}{750k\Omega} - 15\mu A) \times 500ms}{16V}$$

$$= 3.86\mu F$$

Set C_{VIN}

C_{VIN} =20μF

#7 Set COMP pin

Refer to **Internal pre-charge design for quick start up**

Parameters designed			
R_{COMP}	500Ω	$V_{COMP,IC}$	450mV
C_{COMP1}	10nF	C_{COMP2}	100pF

#8 Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k	0.167	N_{PS}	2
V_{REF}	0.3V	I_{OUT}	0.3A

The current sense resistor is

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}$$

$$= \frac{0.167 \times 0.3V \times 2}{0.3A}$$

$$= 0.334\Omega$$

#9 set ZCS pin

Refer to **Line regulati n modification** and **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First identify R_{ZCSU} need for line regulation.

Known conditions at this step			
k_2	68		
Parameters Designed			
R_{ZCSU}	100kΩ		

Then compute R_{ZCSD}

Conditions			
V_{ZCS_OVP}	1.42V	V_{OVP}	48V

V_{OUT}	38V		
Parameters designed			
R_{ZCSU}	100kΩ		
N_S	21	N_{AUX}	5

$$R_{ZCSD} < \frac{\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OUT}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU}$$

$$= \frac{\frac{1.42V}{38V} \times \frac{21}{6}}{1-\frac{1.42V}{38V} \times \frac{21}{6}} \times 100k\Omega$$

$$= 18.62k\Omega$$

$$R_{ZCSD} \geq \frac{\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}}{1-\frac{V_{ZCS\_OVP}}{V_{OVP}} \times \frac{N_S}{N_{AUX}}} \times R_{ZCSU}$$

$$= \frac{\frac{1.42V}{48V} \times \frac{21}{5}}{1-\frac{1.42V}{48V} \times \frac{21}{5}} \times 100k\Omega$$

$$=14.19k\Omega$$

R_{ZCSD} is set to

R_{ZCSD} =15kΩ

#10 set ADM and PWM pin

Refer to **PWM Dimming Mode Design**

Conditions			
$V_{VIN,OFF}$	6V		
Parameters designed			
$R_{ADIM,up}$	200kΩ		

#11 set input bus capacit r

Refer to **Input BUS apacitor (C_{BUS})**

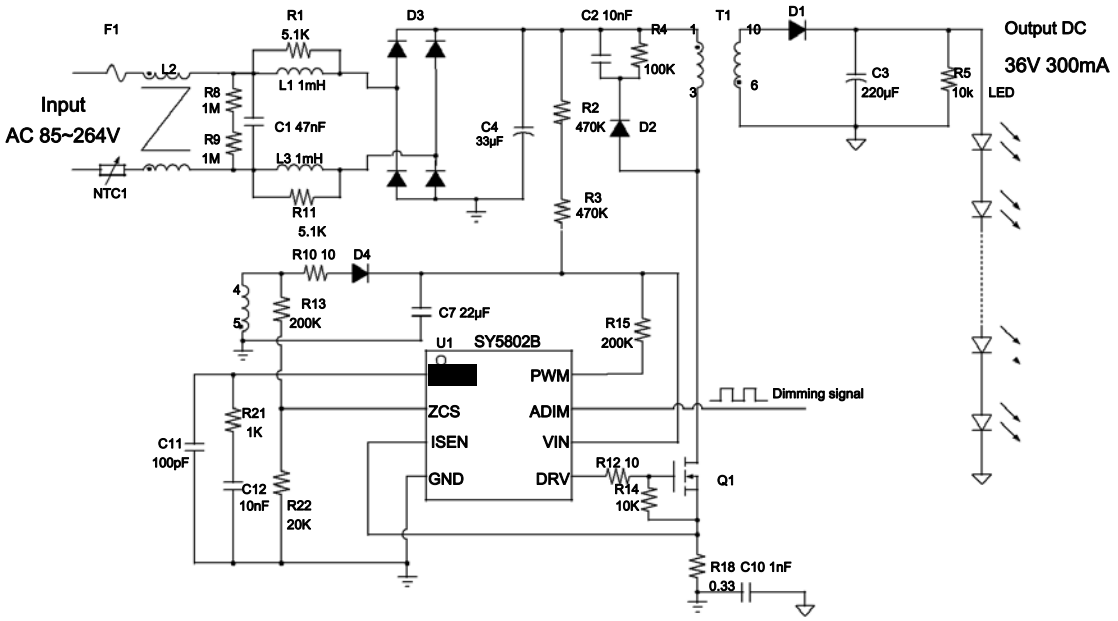
Conditions			
P_{IN}	10.8W	$V_{AC,MIN}$	90V

C_{BUS} =P_{IN} × 3μF/W=10.8W × 3μF/W=32.4μF

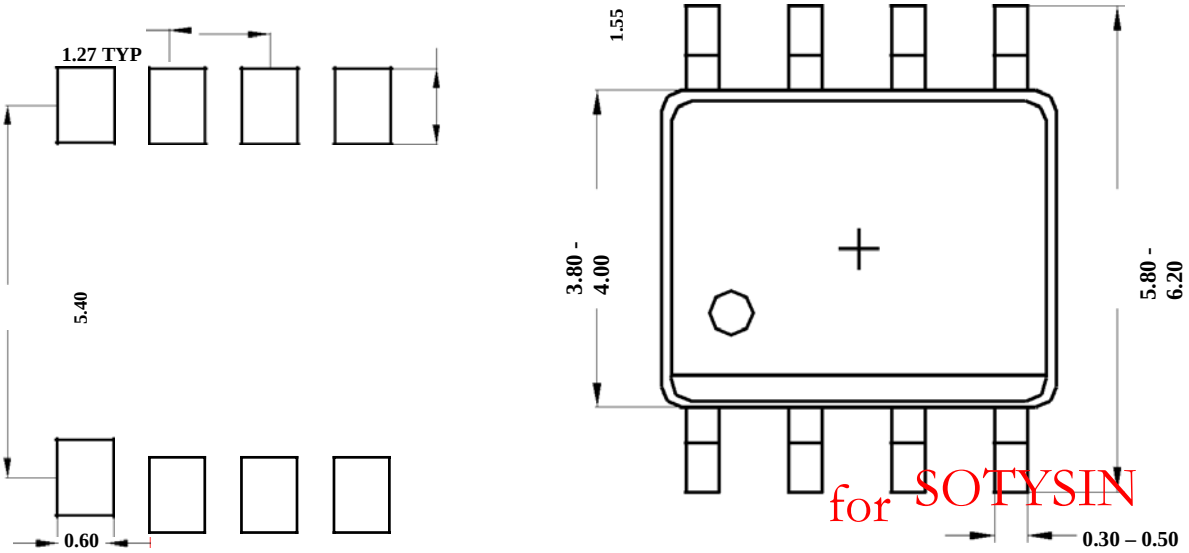
C_{BUS} is set to

C_{BUS}=33μF

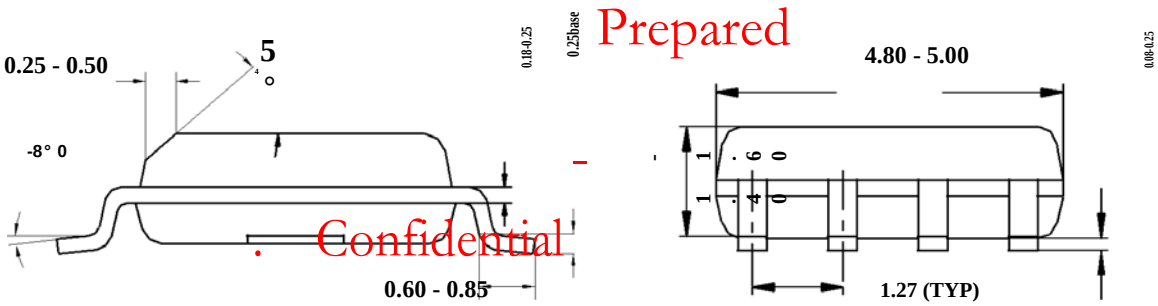
#11 final result


F1
L2
Input
AC 85~264V
NTC1
R8
1M
R9
1M
R1
5.1K
L1 1mH
C1 47nF
L3 1mH
R11
5.1K
D3
C4
33μF
C2 10nF
R4
100K
R2
470K
D2
R3
470K
T1
10
6
1
3
D1
C3
220μF
R5
10k
LED
Output DC
36V 300mA
R10 10
D4
4
5
R13
200K
C7 22μF
U1
SY5802B
R15
200K
PWM
ZCS
ADIM
ISEN
VIN
GND
DRV
Dimming signal
C11
100pF
R21
1K
C12
10nF
R22
20K
R12 10
R14
10K
Q1
R18 C10 1nF
0.33

SO8 Package Outline & PCB Layout Design



Recommended Pad Layout



N tes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.