
11.3-Gbps RATE-SELECTABLE LIMITING AMPLIFIER

FEATURES

- Up to 11.3-Gbps Operation
- 2-Wire Digital Interface
- Digitally Selectable Input Bandwidth
- Adjustable LOS Threshold
- Digitally Selectable Output Voltage
- Digitally Selectable Output Pre-Emphasis
- Adjustable Input Threshold Voltage
- Low Power Consumption
- Input Offset Cancellation
- CML Data Outputs with On-Chip 50-Ω Back-Termination to VCC
- Single +3.3-V Supply

- Output Disable
- Surface Mount Small Footprint 3mm × 3mm 16-Pin RoHS compliant QFN Package

APPLICATIONS

- 10-Gigabit Ethernet Optical Receivers
- 2x/4x/8x and 10x Fiber Channel Optical Receivers
- SONET OC-192/SDH-64 Optical Receivers
- SFP+ and XFP Transceiver Modules
- XENPAK, XPAK, X2 and 300-pin MSA Transponder Modules
- Cable Driver and Receiver

DESCRIPTION

The ONET8501PB is a high-speed, 3.3-V limiting amplifier for multiple fiber optic and copper cable applications with data rates from 2 Gbps up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the bandwidth, output amplitude, output pre-emphasis, input threshold voltage (slice level) and the loss of signal assert level. Predetermined settings for bandwidth and LOS assert levels can also be selected with external rate selection pins.

The ONET8501PB provides a gain of about 34dB which ensures a fully differential output swing for input signals as low as 20mV_{p-p}. The output amplitude can be adjusted to 350mV_{pp}, 650mV_{pp}, or 850mV_{pp}. To compensate for frequency dependent loss of microstrips or striplines connected to the output of the device, programmable pre-emphasis is included in the output stage. A settable loss of signal detection and output disable are also provided.

The device, available in RoHS compliant small footprint 3mm × 3mm 16-pin QFN package, typically dissipates less than 170 mW and is characterized for operation from –40°C to 100°C.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

A simplified block diagram of the ONET8501PB is shown in Figure 1.

This compact, low power 11.3 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block (DC feedback) combined with an analog settable input threshold adjust, a loss of signal detection block using 2 peak detectors, a two-wire interface with a control-logic block and a bandgap voltage reference and bias current generation block.

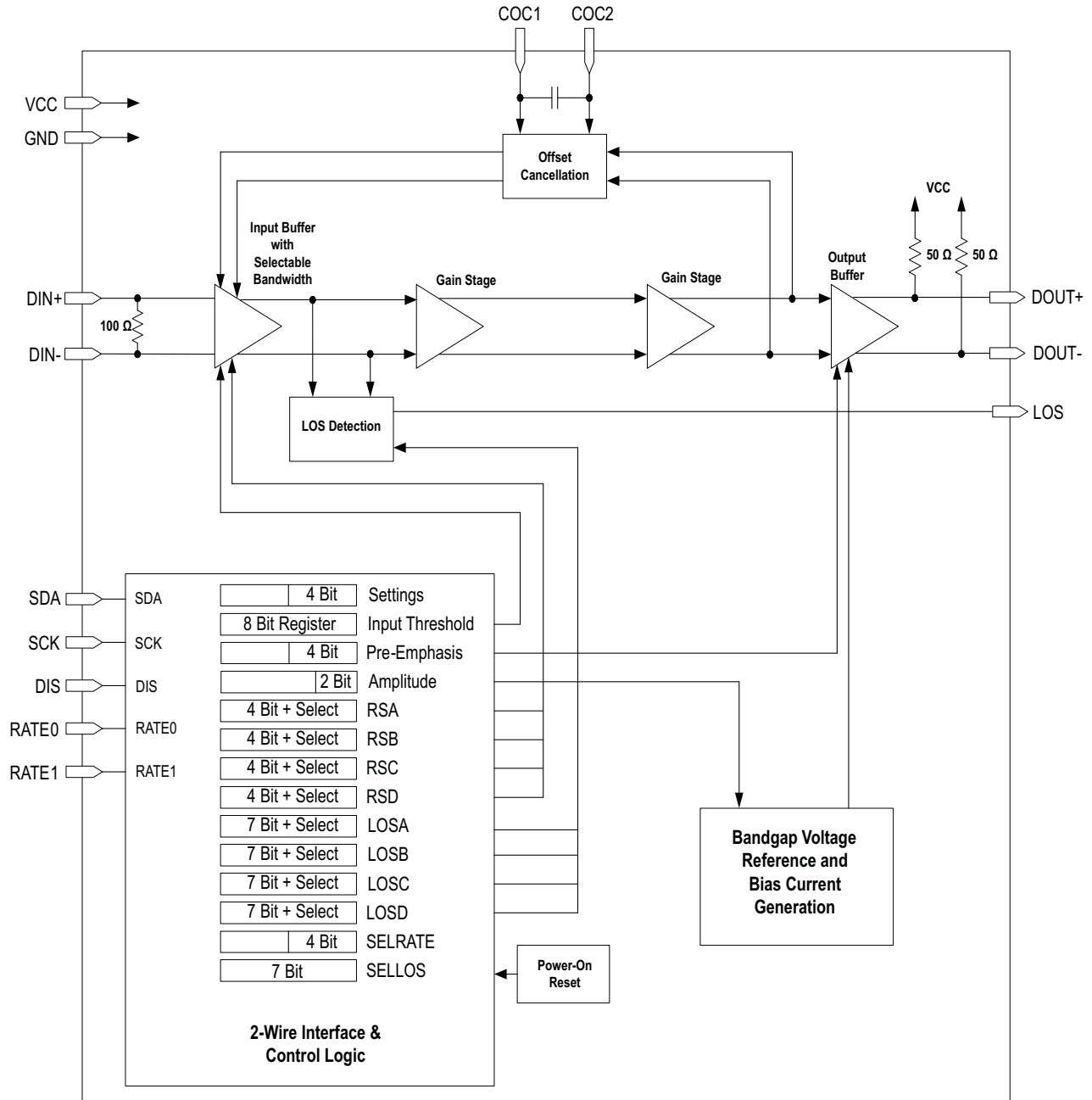


Figure 1. Simplified Block Diagram of the ONET8501PB

PACKAGE

The ONET8501PB is available in a small footprint 3mm × 3mm 16-pin RoHS compliant QFN package with a lead pitch of 0,5 mm. The pin out is shown in [Figure 2](#).

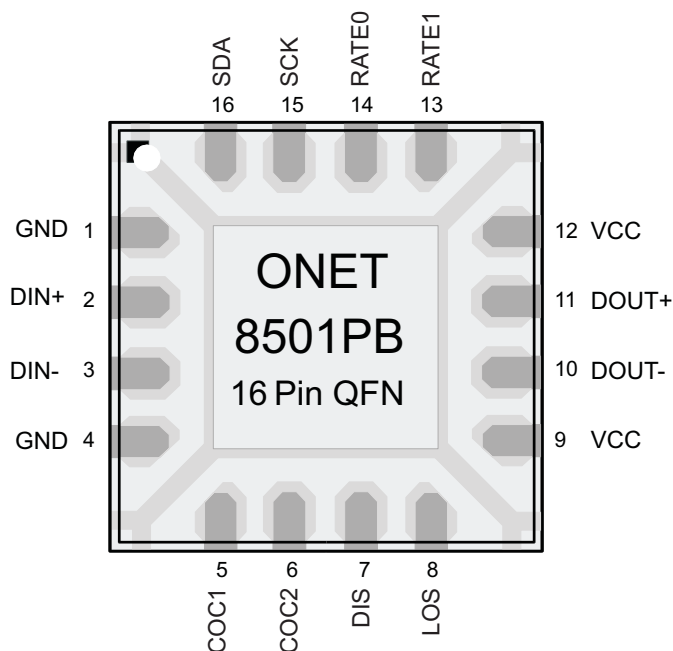


Figure 2. Pinout of ONET8501PB in a 3mm × 3mm 16-Pin QFN package (top view)

PIN DESCRIPTION

| NO. | NAME | TYPE | DESCRIPTION |
|---------|-------|----------------|--|
| 1,4, EP | GND | Supply | Circuit ground. Exposed die pad (EP) must be grounded. |
| 2 | DIN+ | Analog-input | Non-inverted data input. Differentially 100 Ω terminated to DIN–. |
| 3 | DIN– | Analog-input | Inverted data input. Differentially 100 Ω terminated to DIN+. |
| 5 | COC1 | Analog | Offset cancellation filter capacitor plus terminal. An external capacitor can be connected between this pin and COC2 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together. |
| 6 | COC2 | Analog | Offset cancellation filter capacitor minus terminal. An external capacitor can be connected between this pin and COC1 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together. |
| 7 | DIS | Digital-input | Disables the output stage when set to a high level. |
| 8 | LOS | Open drain MOS | High level indicates that the input signal amplitude is below the programmed threshold level. Open drain output. Requires an external 10-kΩ pull-up resistor to VCC for proper operation. |
| 9, 12 | VCC | Supply | 3.3-V ± 10% supply voltage. |
| 10 | DOUT– | CML-out | Inverted data output. On-chip 50 Ω back-terminated to VCC. |
| 11 | DOUT+ | CML-out | Non-inverted data output. On-chip 50 Ω back-terminated to VCC. |
| 13 | RATE1 | Digital-input | Bandwidth selection for noise suppression. |
| 14 | RATE0 | Digital-input | Bandwidth selection for noise suppression. |
| 15 | SCK | Digital-input | Serial interface clock input. Connect a pull-up resistor (10 kΩ typical) to VCC. |
| 16 | SDA | Digital-input | Serial interface data input. Connect a pull-up resistor (10 kΩ typical) to VCC. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|--|---|-------------|----------|
| V_{CC} | Supply voltage ⁽²⁾ | –0.3 to 4.0 | V |
| V_{DIN+} , V_{DIN-} | Voltage at DIN+, DIN– ⁽²⁾ | 0.5 to 4.0 | V |
| V_{LOS} , V_{COC1} , V_{COC2} , V_{DOUT+} , V_{DOUT-} , V_{DIS} , V_{RATE0} , V_{RATE1} , V_{SDA} , V_{SCK} | Voltage at LOS, COC1, COC2, DOUT+, DOUT–, DIS, RATE0, RATE1, SDA, SCK ⁽²⁾ | –0.3 to 4.0 | V |
| $V_{DIN,DIFF}$ | Differential voltage between DIN+ and DIN– | ±2.5 | V |
| I_{DIN+} , I_{DIN-} , I_{DOUT+} , I_{DOUT-} | Continuous current at inputs and outputs | 25 | mA |
| ESD | ESD rating at all pins | 2 | kV (HBM) |
| $T_{J,max}$ | Maximum junction temperature | 125 | °C |
| T_A | Characterized free-air operating temperature range | –40 to 100 | °C |
| T_{STG} | Storage temperature range | –65 to 150 | °C |
| T_{LEAD} | Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device exposure to conditions outside the Absolute Maximum Ratings ranges for an extended duration can affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|------|-----|-----|------|
| V_{CC} | Supply voltage | 2.95 | 3.3 | 3.6 | V |
| T_A | Operating free-air temperature | –40 | | 100 | °C |
| | DIGITAL input high voltage | 2.0 | | | V |
| | DIGITAL input low voltage | | | 0.8 | V |

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, outputs connected to a 50-Ω load, AMP1 = 0, AMP0 = 1 (Register 3) unless otherwise noted. Typical operating condition is at $V_{CC} = 3.3$ V and $T_A = 25$ °C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|------|-----|-----|------|
| V_{CC} | Supply voltage | 2.95 | 3.3 | 3.6 | V |
| I_{VCC} | Supply current DIS = 0, CML currents included | | 50 | 63 | mA |
| R_{IN} | Data input resistance Differential | | 100 | | Ω |
| R_{OUT} | Data output resistance Single-ended, referenced to V_{CC} | | 50 | | Ω |
| | LOS HIGH voltage $I_{SOURCE} = 50$ μA with 10 kΩ pull-up to V_{CC} | 2.4 | | | V |
| | LOS LOW voltage $I_{SINK} = 10$ mA with 10 kΩ pull-up to V_{CC} | | | 0.4 | V |

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, outputs connected to a 50-Ω load, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted. Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|----------------|---|---|------|--------------------|------|-------------------|
| f_{3dB-H} | –3dB bandwidth default settings | RATE1 = 1, RATE0 = 0 | 7.5 | 9.0 | | GHz |
| | | RATE1 = 1, RATE0 = 1 | | 8.4 | | |
| | | RATE1 = 0, RATE0 = 1 | | 7.6 | | |
| | | RATE1 = 0, RATE0 = 0 | | 2.4 | | |
| f_{3dB-L} | Low frequency –3dB bandwidth | With 330-pF COC capacitor | | 10 | 45 | kHz |
| $V_{IN,MIN}$ | Data input sensitivity | PRBS31 pattern at 11.3 Gbps, BER < 10^{-12} | | 5 | 9 | mV _{pp} |
| | | $V_{OD,min} \geq 0.95 \times V_{OD}$ (output limited) | | 20 | 30 | |
| | | PRBS31 pattern at 8.5 Gbps, BER < 10^{-12} , RATE1 = 1, RATE0 = 0 | | 4 | | |
| | | PRBS31 pattern at 4.25 Gbps, BER < 10^{-12} , RATE1 = 1, RATE0 = 1 | | 4 | | |
| | | PRBS31 pattern at 2.125 Gbps, BER < 10^{-12} , RATE1 = 0, RATE0 = 1 | | 4 | | |
| SDD11 | Differential input return gain | 0.01 GHz < f < 3.9 GHz | | | –16 | dB |
| | | 3.9 GHz < f < 12.1 GHz | | See ⁽¹⁾ | | |
| SDD22 | Differential output return gain | 0.01 GHz < f < 3.9 GHz | | | –16 | dB |
| | | 3.9 GHz < f < 12.1 GHz | | See ⁽¹⁾ | | |
| SCD11 | Differential to common mode conversion gain | 0.01 GHz < f < 12.1 GHz | | | –15 | dB |
| SCC22 | Common mode output return gain | 0.01 GHz < f < 7.5 GHz | | | –13 | dB |
| | | 7.5 GHz < f < 12.1 GHz | | | –9 | |
| A | Small signal gain | | 29 | 34 | | dB |
| $V_{IN,MAX}$ | Data input overload | | 2000 | | | mV _{pp} |
| DJ | Deterministic jitter at 11.3 Gbps | $V_{IN} = 15\text{ mV}_{pp}$, K28.5 pattern | | 3 | 8 | pS _{pp} |
| | | $V_{IN} = 30\text{ mV}_{pp}$, K28.5 pattern | | 3 | 10 | |
| | | $V_{IN} = 2000\text{ mV}_{pp}$, K28.5 pattern | | 6 | 15 | |
| | Deterministic jitter at 8.5 Gbps | $V_{IN} = 30\text{ mV}_{pp}$, K28.5 pattern, RATE1 = 1, RATE0 = 0 | | 4 | | pS _{pp} |
| | Deterministic jitter at 4.25 Gbps | $V_{IN} = 30\text{ mV}_{pp}$, K28.5 pattern, RATE1 = 1, RATE0 = 1 | | 6 | | pS _{pp} |
| | Deterministic jitter at 2.125 Gbps | $V_{IN} = 30\text{ mV}_{pp}$, K28.5 pattern, RATE1 = 0, RATE0 = 1 | | 8 | | pS _{pp} |
| RJ | Random jitter | $V_{IN} = 30\text{ mV}_{pp}$ | | 1 | | pS _{rms} |
| V_{OD} | Differential data output voltage | $V_{IN} > 30\text{ mV}_{pp}$, DIS = 0, AMP1 = 0, AMP0 = 0 | 250 | 350 | 450 | mV _{pp} |
| | | $V_{IN} > 30\text{ mV}_{pp}$, DIS = 0, AMP1 = 0, AMP0 = 1 | 500 | 650 | 800 | |
| | | $V_{IN} > 30\text{ mV}_{pp}$, DIS = 0, AMP1 = 1, AMP0 = 1 | 650 | 850 | 1050 | |
| | | DIS = 1 | | | 5 | mV _{rms} |
| V_{PREEM} | Output pre-emphasis step size | | | 1 | | dB |
| t_R | Output rise time | 20% to 80%, $V_{IN} > 30\text{ mV}_{pp}$ | | 28 | 40 | ps |
| t_F | Output fall time | 20% to 80%, $V_{IN} > 30\text{ mV}_{pp}$ | | 28 | 40 | ps |
| CMOV | AC Common mode output voltage | PRBS31 pattern; AMP1 = 0, AMP0 = 1 | | | 7 | mV _{rms} |
| V_{TH} | LOW LOS assert threshold range min | K28.5 pattern at 11.3 Gbps, LOSRNG = 0 | | 15 | | mV _{pp} |
| | LOW LOS assert threshold range max | K28.5 pattern at 11.3 Gbps, LOSRNG = 0 | | 35 | | |
| V_{TH} | HIGH LOS assert threshold range min | K28.5 pattern at 11.3 Gbps, LOSRNG = 1 | | 35 | | mV _{pp} |
| | HIGH LOS assert threshold range max | K28.5 pattern at 11.3 Gbps, LOSRNG = 1 | | 80 | | |
| | LOS threshold variation | Versus temperature at 11.3 Gbps | | 1.5 | | dB |
| | | Versus supply voltage V_{CC} at 11.3 Gbps | | 1 | | dB |
| | | Versus data rate | | 1.5 | | dB |
| | LOS hysteresis (electrical) | K28.5 pattern at 11.3 Gbps | 2 | 4 | 6 | dB |
| T_{LOS_AST} | LOS assert time | | 2.5 | 10 | 80 | μs |
| T_{LOS_DEA} | LOS deassert time | | 2.5 | 10 | 80 | μs |

(1) Differential Return Gain given by SDD11, SDD22 = $-11.6 + 13.33 \log_{10}(f/8.25)$, f in GHz

AC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, outputs connected to a 50-Ω load, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted. Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------|-----------------------|----------------|-----|-----|-----|------|
| T_{DIS} | Disable response time | | | 20 | | ns |

DETAILED DESCRIPTION

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of input signal pins DIN+ / DIN–. The data path consists of a 100Ω differential termination resistor followed by a digitally controlled bandwidth switch input buffer for rate select. The RATE1 and RATE0 pins can be used to control the bandwidth of the filter. Default bandwidth settings are used; however, these can be changed using registers 4 through 7 via the serial interface. For details regarding the rate selection, see [Table 19](#). A gain stage and an output buffer stage follow the input buffer, which together provide a gain of 34dB. The device can accept input amplitude levels from 5mV_{pp} up to 2000mV_{pp}. The amplified data output signal is available at the output pins DOUT+ / DOUT– which include on-chip 2 × 50Ω back-termination to VCC.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. The offset cancellation can be disabled so that the input threshold voltage can be adjusted to optimize the bit error rate or change the eye crossing to compensate for input signal pulse width distortion. The offset cancellation can be disabled by setting OCDIS = 1 (bit 1 of register 0). The input threshold level can be adjusted using register settings THADJ[0..7] (register 1). For details regarding input threshold adjust, see [Table 19](#).

The low frequency cutoff is as low as 80kHz with the built-in filter capacitor. For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1 and COC2 pins. A value of 330pF results in a low frequency cutoff of 10kHz.

BANDGAP VOLTAGE AND BIAS GENERATION

The ONET8501PB limiting amplifier is supplied by a single +3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

HIGH-SPEED OUTPUT BUFFER

The output amplitude of the buffer can be set to 350 mV_{pp}, 650 mV_{pp} or 850 mV_{pp} using register settings AMP[0..1] (register 3) via the serial interface. To compensate for frequency dependant losses of transmission lines connected to the output, the ONET8501PB has adjustable pre-emphasis of the output stage. The pre-emphasis can be set from 0 to 8 dB in 1 dB steps using register settings PEADJ[0..3] (register 2).

RATE SELECT

There are 16 possible internal filter settings (4 bit) to adjust the small signal bandwidth to the data rate. For fast rate selection, 4 default values can be selected with the RATE1 and RATE0 pins. Using the serial interface, the bandwidth settings can be customized instead of using the default values. The default bandwidths and the registers used to change the bandwidth settings are shown in [Table 1](#).

Table 1. Rate Selection Default Settings and Registers Used for Adjustment

| RATE1 | RATE0 | DEFAULT BANDWIDTH (GHz) | REGISTER USED FOR ADJUSTMENT |
|-------|-------|-------------------------|------------------------------|
| 0 | 0 | 2.4 | RSA (Register 4) |
| 0 | 1 | 7.6 | RSB (Register 5) |
| 1 | 1 | 8.4 | RSC (Register 6) |
| 1 | 0 | 9.0 | RSD (Register 7) |

If the rate select register selection bit is set LOW, for example RSASEL = 0 (bit 7 of register 4), then the default bandwidth for that register is used. If the register selection bit is set HIGH, for example RSASEL = 1 (bit 7 of register 4), then the content of RSA[0..3] (register 4) is used to set the input filter bandwidth when RATE0 = 0 and RATE1 = 0. The settings of the rate selection registers RSA, RSB, RSC and RSD and the corresponding filter bandwidths are shown in [Table 2](#).

Table 2. Available Bandwidth Settings

| RSX3 | RSX2 | RSX1 | RSX0 | TYPICAL BANDWIDTH (GHz) |
|------|------|------|------|-------------------------|
| 0 | 0 | 0 | 0 | 9.0 |
| 0 | 0 | 0 | 1 | 8.6 |
| 0 | 0 | 1 | 0 | 8.4 |
| 0 | 0 | 1 | 1 | 8.1 |
| 0 | 1 | 0 | 0 | 7.9 |
| 0 | 1 | 0 | 1 | 7.6 |
| 0 | 1 | 1 | 0 | 6.9 |
| 0 | 1 | 1 | 1 | 6.2 |
| 1 | 0 | 0 | 0 | 5.2 |
| 1 | 0 | 0 | 1 | 4.2 |
| 1 | 0 | 1 | 0 | 3.7 |
| 1 | 0 | 1 | 1 | 3.4 |
| 1 | 1 | 0 | 0 | 3.2 |
| 1 | 1 | 0 | 1 | 2.8 |
| 1 | 1 | 1 | 0 | 2.6 |
| 1 | 1 | 1 | 1 | 2.4 |

The RATE1 and RATE0 pins do not have to be used if the serial interface is being used. If RATE1 is not connected it is internally pulled HIGH and if RATE0 is not connected it is internally pulled LOW, thus selecting register 7. Therefore, changing the contents of RSD[0..3] (register 7) through the serial interface can be used to adjust the bandwidth.

LOSS OF SIGNAL DETECTION

The loss of signal detection is done by 2 separate level detectors to cover a wide dynamic range. The peak values of the input signal and the output signal of the gain stage are monitored by the peak detectors. The peak values are compared to a pre-defined loss of signal threshold voltage inside the loss of signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated. The LOS assert level is settable through the serial interface. There are 2 LOS ranges settable with the LOSRNG bit (bit 2 register 0) via the serial interface. By setting the bit LOSRNG = 1, the high range of the LOS assert values are used (35mV_{PP} to 80mV_{PP}) and by setting the bit LOSRNG = 0, the low range of the LOS assert values are used (15mV_{PP} to 35mV_{PP}).

There are 128 possible internal LOS settings (7 bit) for each LOS range to adjust the LOS assert level. For fast LOS selection, 4 default values can be selected with the RATE1 and RATE0 pins; however, the LOS settings can be customized instead of using the default values. The default LOS assert levels and the registers used to change the LOS settings are shown in [Table 3](#).

Table 3. LOS Assert Level Default Settings and Registers Used for Adjustment

| RATE1 | RATE0 | DEFAULT LOS ASSERT LEVEL (mV _{PP}) | REGISTER USED FOR ADJUSTMENT |
|-------|-------|--|------------------------------|
| 0 | 0 | 15 | LOSA (Register 8) |
| 0 | 1 | 18 | LOSB (Register 9) |
| 1 | 1 | 26 | LOSC (Register 10) |
| 1 | 0 | 26 | LOSD (Register 11) |

If the LOS register selection bit is set low, for example LOSASEL = 0 (bit 7 of register 8), then the default LOS assert level for that register is used. If the register selection bit is set high, for example LOSASEL = 1 (bit 7 of register 8), then the content of LOSA[0..6] (register 8) is used to set the LOS assert level when RATE1 = 0 and RATE0 = 0. The RATE1 and RATE0 pins do not have to be used if the serial interface is being used. If RATE1 is not connected it is internally pulled HIGH and if RATE0 is not connected it is internally pulled LOW, thus selecting register 11. Therefore, changing the content of LOSD[0..6] (register 11) through the serial interface can be used to adjust the LOS assert level.

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET8501PB uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100-k Ω pull-up resistors to VCC. For driving these inputs, an open drain output is recommended.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The ONET8501PB is a slave device only which means that it can not initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (1000100) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET8501PB is I²C compatible. The typical timing is shown in [Figure 3](#) and a complete data transfer is shown in [Figure 4](#). Parameters for [Figure 3](#) are defined in [Table 4](#).

Bus Idle: Both SDA and SCK lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer begins with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer ends with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

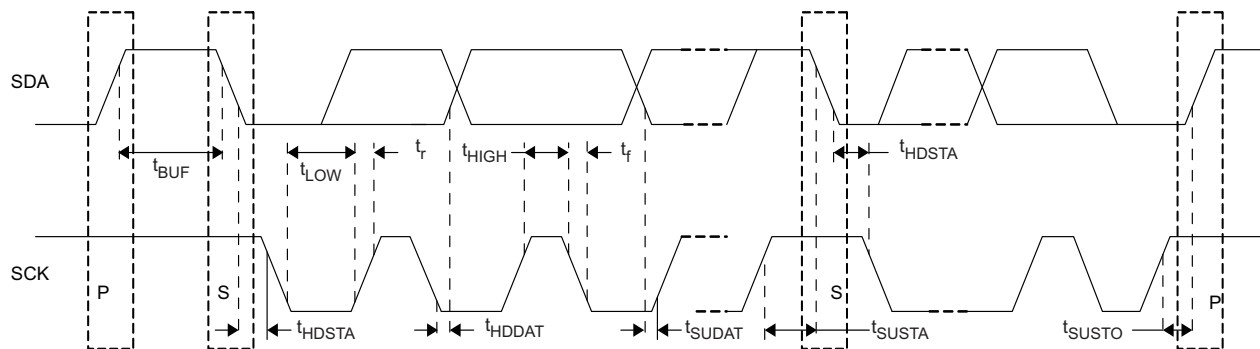


Figure 3. I²C Timing Diagram

Table 4. Timing Diagram Definitions

| PARAMETER | | MIN | MAX | UNIT |
|-------------|---|-----|-----|---------|
| f_{SCK} | SCK clock frequency | | 400 | kHz |
| t_{BUF} | Bus free time between START and STOP conditions | 1.3 | | μ s |
| t_{HDSTA} | Hold time after repeated START condition. After this period, the first clock pulse is generated | 0.6 | | μ s |
| t_{LOW} | Low period of the SCK clock | 1.3 | | μ s |
| t_{HIGH} | High period of the SCK clock | 0.6 | | μ s |
| t_{SUSTA} | Setup time for a repeated START condition | 0.6 | | μ s |
| t_{HDDAT} | Data HOLD time | 0 | | μ s |
| t_{SUDAT} | Data setup time | 100 | | ns |
| t_r | Rise time of both SDA and SCK signals | | 300 | ns |
| t_f | Fall time of both SDA and SCK signals | | 300 | ns |
| t_{SUSTO} | Setup time for STOP condition | 0.6 | | μ s |

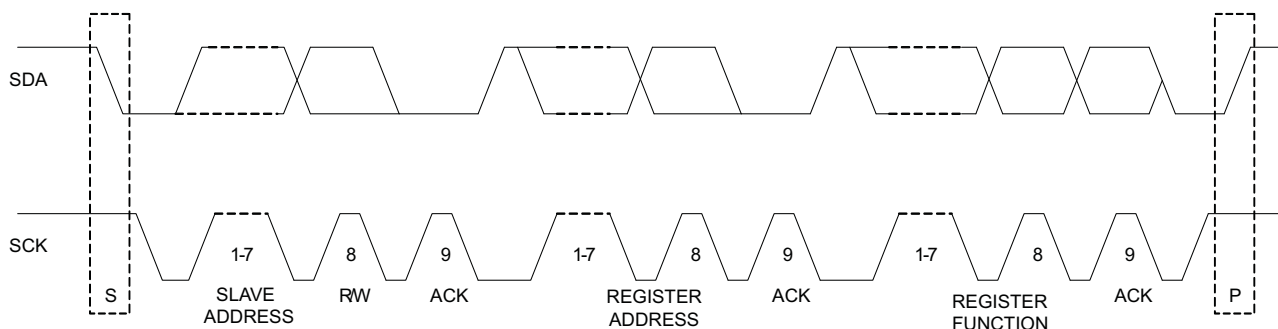


Figure 4. I²C Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 11 (0x0B) are shown in [Table 5](#) through [Table 16](#). The register mapping for the read only register addresses 14 (0x0E) and 15 (0x0F) are shown in [Table 17](#) and [Table 18](#).

[Table 19](#) describes the circuit functionality based on the register settings.

Table 5. Register 0 (0x00) Mapping – Control Settings

| register address 0 (0x00) | | | | | | | |
|---------------------------|-------|-------|------|-------|--------|-------|--------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| – | – | – | – | DIS | LOSRNG | OCDIS | I2CDIS |

Table 6. Register 1 (0x01) Mapping – Input Threshold Adjust

| register address 1 (0x01) | | | | | | | |
|---------------------------|--------|--------|--------|--------|--------|--------|--------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| THADJ7 | THADJ6 | THADJ5 | THADJ4 | THADJ3 | THADJ2 | THADJ1 | THADJ0 |

Table 7. Register 2 (0x02) Mapping – Pre-emphasis Adjust

| register address 2 (0x02) | | | | | | | |
|---------------------------|-------|-------|------|--------|--------|--------|--------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| – | – | – | – | PEADJ3 | PEADJ2 | PEADJ1 | PEADJ0 |

Table 8. Register 3 (0x03) Mapping – Output Amplitude Adjust

| register address 3 (0x03) | | | | | | | |
|---------------------------|-------|-------|------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| – | – | – | – | – | – | AMP1 | AMP0 |

Table 9. Register 4 (0x04) Mapping – Rate Selection Register A

| register address 4 (0x04) | | | | | | | |
|---------------------------|-------|-------|------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| RSASEL | – | – | – | RSA3 | RSA2 | RSA1 | RSA0 |

Table 10. Register 5 (0x05) Mapping – Rate Selection Register B

| register address 5 (0x05) | | | | | | | |
|---------------------------|-------|-------|------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| RSBSEL | – | – | – | RSB3 | RSB2 | RSB1 | RSB0 |

Table 11. Register 6 (0x06) Mapping – Rate Selection Register C

| register address 6 (0x06) | | | | | | | |
|---------------------------|-------|-------|------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| RSCSEL | – | – | – | RSC3 | RSC2 | RSC1 | RSC0 |

Table 12. Register 7 (0x07) Mapping – Rate Selection Register D

| register address 7 (0x07) | | | | | | | |
|---------------------------|-------|-------|------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| RSDSEL | – | – | – | RSD3 | RSD2 | RSD1 | RSD0 |

Table 13. Register 8 (0x08) Mapping – LOS Assert Level Register A

| register address 8 (0x08) | | | | | | | |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| LOSASEL | LOSA6 | LOSA5 | LOSA4 | LOSA3 | LOSA2 | LOSA1 | LOSA0 |

Table 14. Register 9 (0x09) Mapping – LOS Assert Level Register B

| register address 9 (0x09) | | | | | | | |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| LOSBSSEL | LOSB6 | LOSB5 | LOSB4 | LOSB3 | LOSB2 | LOSB1 | LOSB0 |

Table 15. Register 10 (0x0A) Mapping – LOS Assert Level Register C

| register address 10 (0x0A) | | | | | | | |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| LOSCSEL | LOSC6 | LOSC5 | LOSC4 | LOSC3 | LOSC2 | LOSC1 | LOSC0 |

Table 16. Register 11 (0x0B) Mapping – LOS Assert Level Register D

| register address 11 (0x0B) | | | | | | | |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| LOSDSEL | LOSD6 | LOSD5 | LOSD4 | LOSD3 | LOSD2 | LOSD1 | LOSD0 |

Table 17. Register 14 (0x0E) Mapping – Selected Rate Setting (Read Only)

| register address 14 (0x0E) | | | | | | | |
|----------------------------|-------|-------|------|----------|----------|----------|----------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| – | – | – | – | SELRATE3 | SELRATE2 | SELRATE1 | SELRATE0 |

Table 18. Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)

| register address 15 (0x0F) | | | | | | | |
|----------------------------|---------|---------|---------|---------|---------|---------|---------|
| bit 7 | bit 6 | bit 5 | bit4 | bit 3 | bit 2 | bit 1 | bit 0 |
| – | SELLOS6 | SELLOS5 | SELLOS4 | SELLOS3 | SELLOS2 | SELLOS1 | SELLOS0 |

Table 19. Register Functionality

| SYMBOL | REGISTER BIT | FUNCTION |
|--------|-----------------------------------|--|
| DIS | Output disable bit 3 | Output disable bit: 1 = output disabled 0 = output enabled |
| LOSRNG | LOS Range bit 2 | LOS range bit: 1 = high LOS assert voltage range 0 = low LOS assert voltage range |
| OCDIS | Offset cancellation disable bit 1 | Offset cancellation disable bit: 1 = offset cancellation is disabled 0 = offset cancellation is enabled |
| I2CDIS | I ² C disable bit 0 | I²C disable bit: 1 = I ² C is disabled. 0 = I ² C is enabled. This is the default setting. |

Table 19. Register Functionality (continued)

| SYMBOL | REGISTER BIT | FUNCTION | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|------------------------------------|--|--|--|-------------------|------------------|---|------|---|------|---|------|---|------|---|------|---|------|---|------|---|------|---|------|
| THADJ7 | Input threshold adjust bit 7 (MSB) | Input threshold adjustment setting: Maximum positive shift for 00000001 (1) Minimum positive shift for 01111111 (127) Zero shift for 10000000 (128) Minimum negative shift for 10000001 (129) Maximum negative shift for 11111111 (255) | | | | | | | | | | | | | | | | | | | | | | |
| THADJ6 | Input threshold adjust bit 6 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ5 | Input threshold adjust bit 5 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ4 | Input threshold adjust bit 4 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ3 | Input threshold adjust bit 3 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ2 | Input threshold adjust bit 2 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ1 | Input threshold adjust bit 1 | | | | | | | | | | | | | | | | | | | | | | | |
| THADJ0 | Input threshold adjust bit 0 (LSB) | | | | | | | | | | | | | | | | | | | | | | | |
| PEADJ3 | Pre-emphasis adjust bit 3 (MSB) | Pre-emphasis setting: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Pre-emphasis (dB)</th> <th>Register Setting</th> </tr> </thead> <tbody> <tr><td>0</td><td>0000</td></tr> <tr><td>1</td><td>0001</td></tr> <tr><td>2</td><td>0011</td></tr> <tr><td>3</td><td>0100</td></tr> <tr><td>4</td><td>0101</td></tr> <tr><td>5</td><td>0111</td></tr> <tr><td>6</td><td>1100</td></tr> <tr><td>7</td><td>1101</td></tr> <tr><td>8</td><td>1111</td></tr> </tbody> </table> | | | Pre-emphasis (dB) | Register Setting | 0 | 0000 | 1 | 0001 | 2 | 0011 | 3 | 0100 | 4 | 0101 | 5 | 0111 | 6 | 1100 | 7 | 1101 | 8 | 1111 |
| Pre-emphasis (dB) | Register Setting | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0000 | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0001 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0011 | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0100 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 0101 | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 0111 | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 1100 | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 1101 | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 1111 | | | | | | | | | | | | | | | | | | | | | | | |
| PEADJ2 | Pre-emphasis adjust bit 2 | | | | | | | | | | | | | | | | | | | | | | | |
| PEADJ1 | Pre-emphasis adjust bit 1 | | | | | | | | | | | | | | | | | | | | | | | |
| PEADJ0 | Pre-emphasis adjust bit 0 (LSB) | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | | | | | | | | | | | | | | | | | | | | | |
| AMP1 | Output amplitude adjustment bit 1 | Output amplitude adjustment: 00 = 350 mV _{pp} 01 = 650 mV _{pp} 10 = 650 mV _{pp} 11 = 850 mV _{pp} | | | | | | | | | | | | | | | | | | | | | | |
| AMP0 | Output amplitude adjustment bit 0 | | | | | | | | | | | | | | | | | | | | | | | |
| RSASEL | Register RSA select bit 7 (MSB) | Rate selection register A RSASEL = 1 Content of register A bits 3 to 0 is used to select the input filter BW RSASEL = 0 Default BW of 2.4 GHz is used Register RSA is used when RATE1 = 0 and RATE0 = 0 | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| RSA3 | Rate select register A bit 3 | | | | | | | | | | | | | | | | | | | | | | | |
| RSA2 | Rate select register A bit 2 | | | | | | | | | | | | | | | | | | | | | | | |
| RSA1 | Rate select register A bit 1 | | | | | | | | | | | | | | | | | | | | | | | |
| RSA0 | Rate select register A bit 0 (LSB) | | | | | | | | | | | | | | | | | | | | | | | |
| RSBSEL | Register RSB select bit 7 (MSB) | Rate selection register B RSBSEL = 1 Content of register B bits 3 to 0 is used to select the input filter BW RSBSEL = 0 Default BW of 7.6 GHz is used Register RSB is used when RATE1 = 0 and RATE0 = 1 | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| – | | | | | | | | | | | | | | | | | | | | | | | | |
| RSB3 | Rate select register B bit 3 | | | | | | | | | | | | | | | | | | | | | | | |
| RSB2 | Rate select register B bit 2 | | | | | | | | | | | | | | | | | | | | | | | |
| RSB1 | Rate select register B bit 1 | | | | | | | | | | | | | | | | | | | | | | | |
| RSB0 | Rate select register B bit 0 (LSB) | | | | | | | | | | | | | | | | | | | | | | | |

Table 19. Register Functionality (continued)

| SYMBOL | REGISTER BIT | FUNCTION |
|---------|---|---|
| RSCSEL | Register RSC select bit 7 (MSB) | Rate selection register C RSCSEL = 1 Content of register C bits 3 to 0 is used to select the input filter BW RSCSEL = 0 Default BW of 8.4 GHz is used Register RSC is used when RATE1 = 1 and RATE0 = 1 |
| – | | |
| – | | |
| – | | |
| RSC3 | Rate select register C bit 3 | |
| RSC2 | Rate select register C bit 2 | |
| RSC1 | Rate select register C bit 1 | |
| RSC0 | Rate select register C bit 0 (LSB) | |
| RSDSEL | Register RSD select bit 7 (MSB) | Rate selection register D RSDSEL = 1 Content of register D bits 3 to 0 is used to select the input filter BW RSDSEL = 0 Default BW of 9.0 GHz is used Register RSD is used when RATE1 = 1 and RATE0 = 0 or RATE1 and RATE0 are not connected |
| – | | |
| – | | |
| – | | |
| RSD3 | Rate select register D bit 3 | |
| RSD2 | Rate select register D bit 2 | |
| RSD1 | Rate select register D bit 1 | |
| RSD0 | Rate select register D bit 0 (LSB) | |
| LOSASEL | Register LOSA select bit 7 (MSB) | LOS assert level register A LOSASEL = 1 Content of register A bits 6 to 0 is used to select the LOS assert level Minimum LOS assert level for 0000000 Maximum LOS assert level for 1111111 LOSASEL = 0 Default LOS assert level of 15 mVpp is used Register LOSA is used when RATE1 = 0 and RATE0 = 0 |
| LOSA6 | LOS assert level register A bit 6 | |
| LOSA5 | LOS assert level register A bit 5 | |
| LOSA4 | LOS assert level register A bit 4 | |
| LOSA3 | LOS assert level register A bit 3 | |
| LOSA2 | LOS assert level register A bit 2 | |
| LOSA1 | LOS assert level register A bit 1 | |
| LOSA0 | LOS assert level register A bit 0 (LSB) | |
| LOSBSEL | Register LOSB select bit 7 (MSB) | LOS assert level register B LOSBSEL = 1 Content of register B bits 6 to 0 is used to select the LOS assert level Minimum LOS assert level for 0000000 Maximum LOS assert level for 1111111 LOSBSEL = 0 Default LOS assert level of 18 mVpp is used Register LOSB is used when RATE1 = 0 and RATE0 = 1 |
| LOSB6 | LOS assert level register B bit 6 | |
| LOSB5 | LOS assert level register B bit 5 | |
| LOSB4 | LOS assert level register B bit 4 | |
| LOSB3 | LOS assert level register B bit 3 | |
| LOSB2 | LOS assert level register B bit 2 | |
| LOSB1 | LOS assert level register B bit 1 | |
| LOSB0 | LOS assert level register B bit 0 (LSB) | |
| LOSCSEL | Register LOSC select bit 7 (MSB) | LOS assert level register C LOSCSEL = 1 Content of register C bits 6 to 0 is used to select the LOS assert level Minimum LOS assert level for 0000000 Maximum LOS assert level for 1111111 LOSCSEL = 0 Default LOS assert level of 26 mVpp is used Register LOSC is used when RATE1 = 1 and RATE0 = 1 |
| LOSC6 | LOS assert level register C bit 6 | |
| LOSC5 | LOS assert level register C bit 5 | |
| LOSC4 | LOS assert level register C bit 4 | |
| LOSC3 | LOS assert level register C bit 3 | |
| LOSC2 | LOS assert level register C bit 2 | |
| LOSC1 | LOS assert level register C bit 1 | |
| LOSC0 | LOS assert level register C bit 0 (LSB) | |

Table 19. Register Functionality (continued)

| SYMBOL | REGISTER BIT | FUNCTION |
|----------|---|---|
| LODSEL | Register LOSD select bit 7 (MSB) | LOS assert level register D LODSEL = 1 Content of register D bits 6 to 0 is used to select the LOS assert level Minimum LOS assert level for 0000000 Maximum LOS assert level for 1111111 LODSEL = 0 Default LOS assert level of 26 mVpp is used Register LOSD is used when RATE1 = 1 and RATE0 = 0 |
| LOSD6 | LOS assert level register D bit 6 | |
| LOSD5 | LOS assert level register D bit 5 | |
| LOSD4 | LOS assert level register D bit 4 | |
| LOSD3 | LOS assert level register D bit 3 | |
| LOSD2 | LOS assert level register D bit 2 | |
| LOSD1 | LOS assert level register D bit 1 | |
| LOSD0 | LOS assert level register D bit 0 (LSB) | |
| SELRATE3 | Selected rate setting bit 3 | Selected rate setting (read only) |
| SELRATE2 | Selected rate setting bit 2 | |
| SELRATE1 | Selected rate setting bit 1 | |
| SELRATE0 | Selected rate setting bit 0 | |
| SELLOS6 | Selected LOS assert level bit 6 (MSB) | Selected LOS assert level (read only) |
| SELLOS5 | Selected LOS assert level bit 5 | |
| SELLOS4 | Selected LOS assert level bit 4 | |
| SELLOS3 | Selected LOS assert level bit 3 | |
| SELLOS2 | Selected LOS assert level bit 2 | |
| SELLOS1 | Selected LOS assert level bit 1 | |
| SELLOS0 | Selected LOS assert level bit 0 (LSB) | |

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted.

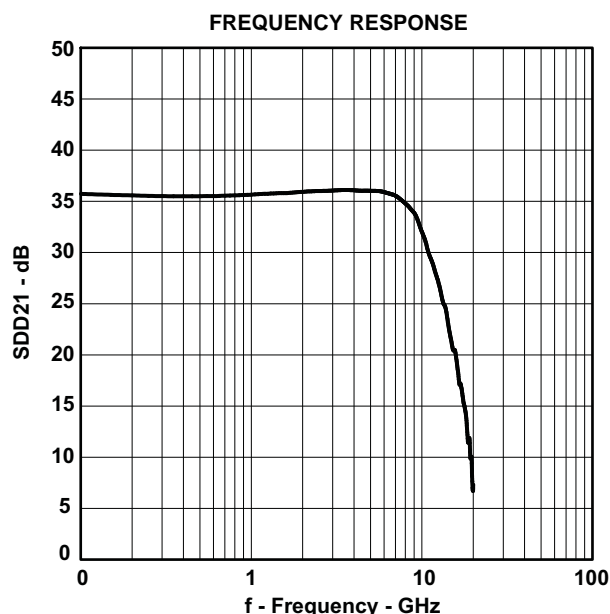


Figure 5.

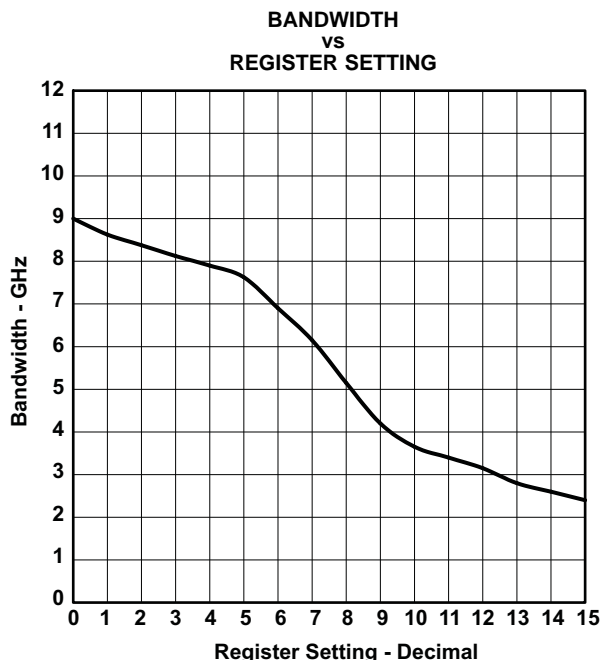


Figure 6.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted.

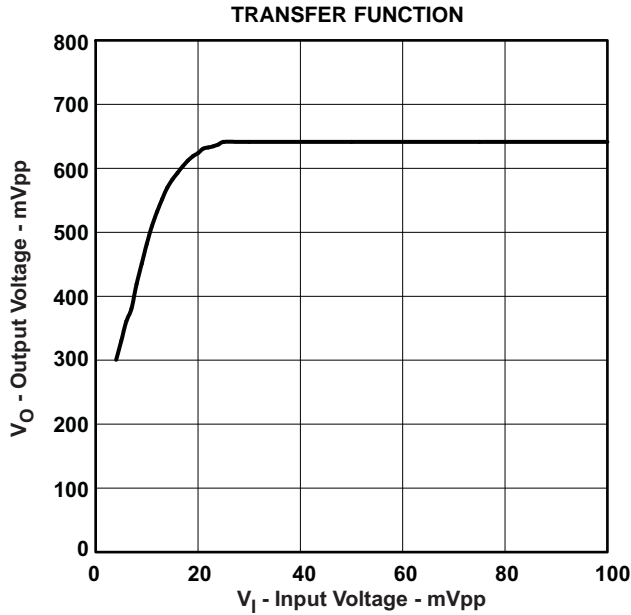


Figure 7.

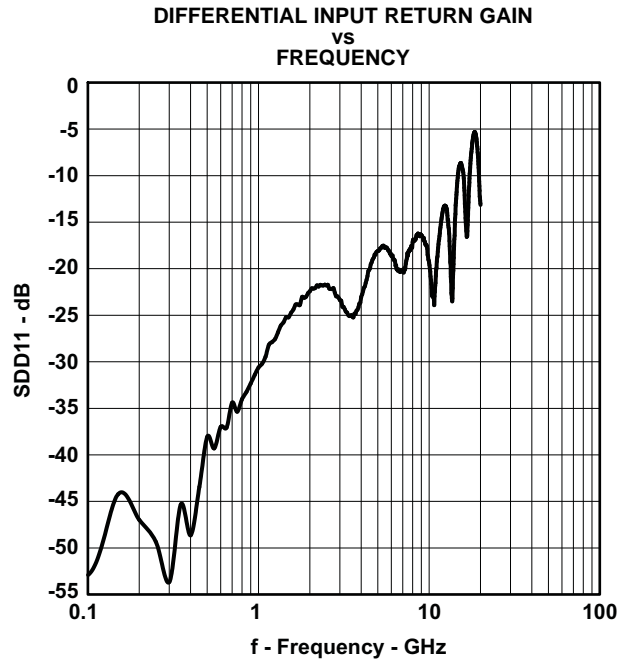


Figure 8.

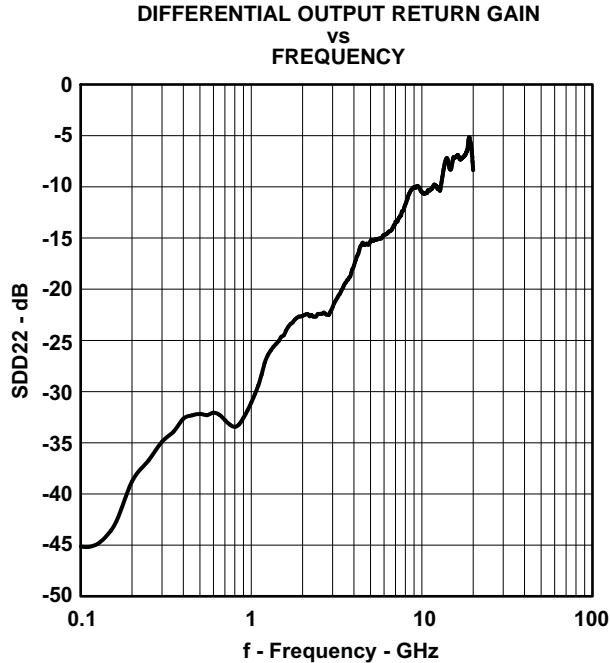


Figure 9.

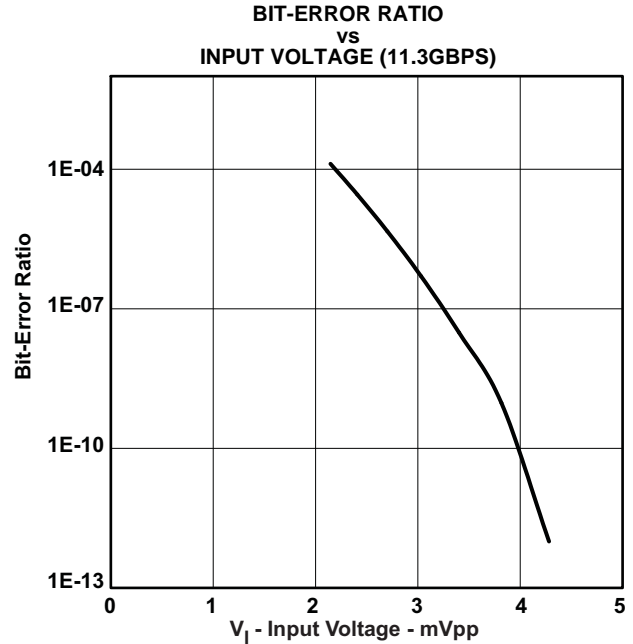


Figure 10.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted.

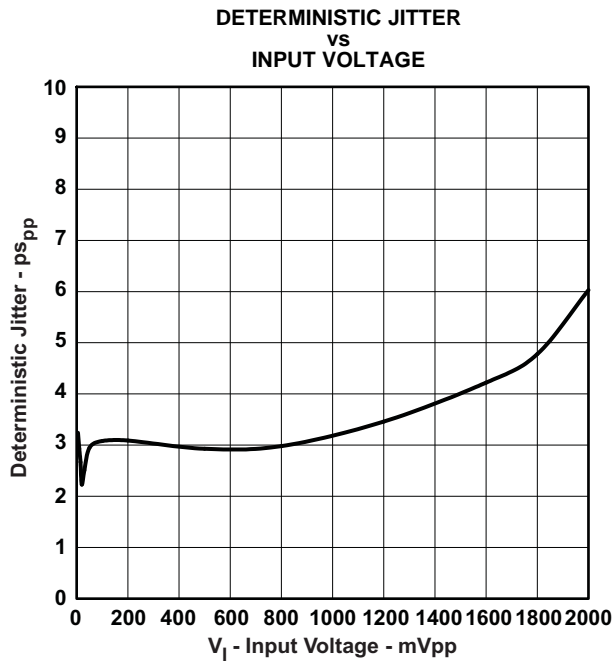


Figure 11.

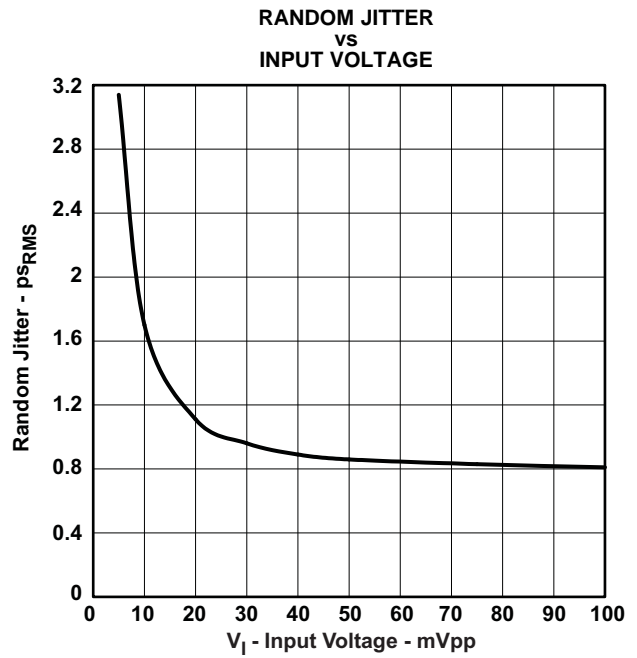


Figure 12.

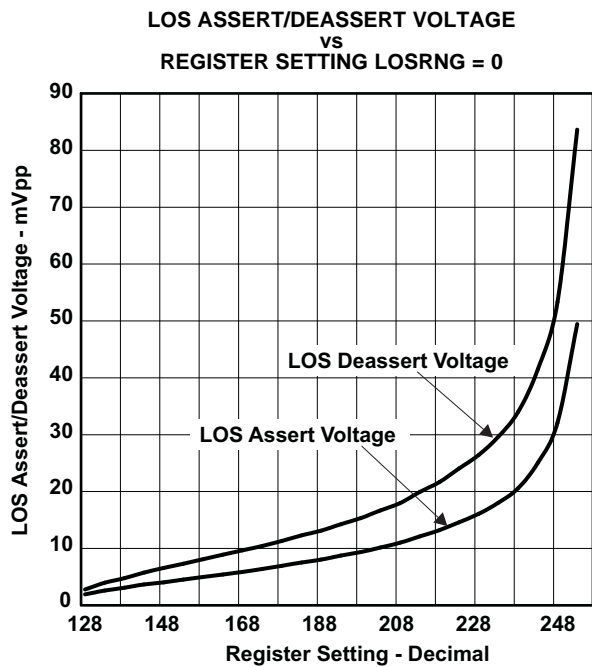


Figure 13.

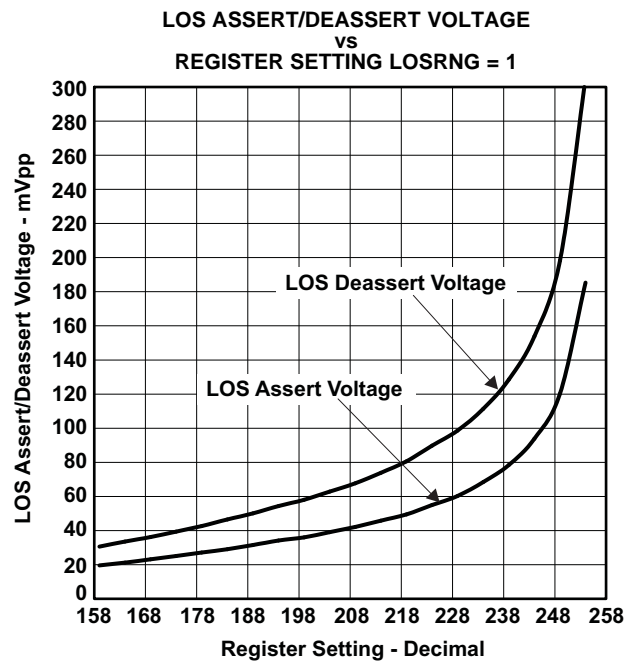


Figure 14.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted.

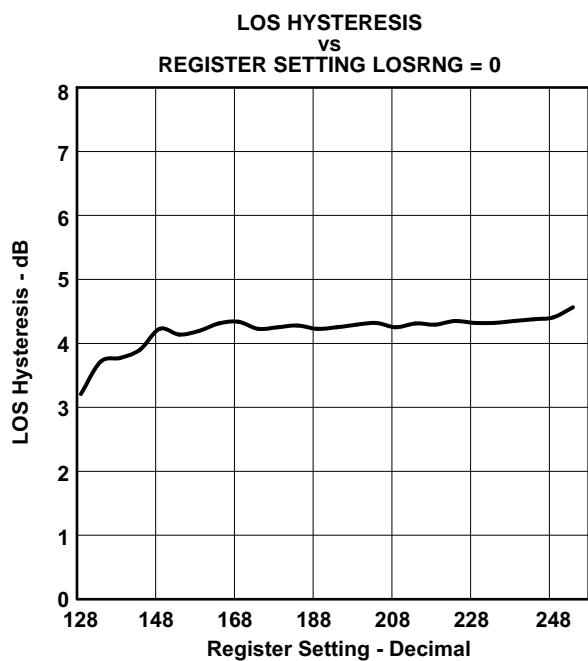


Figure 15.

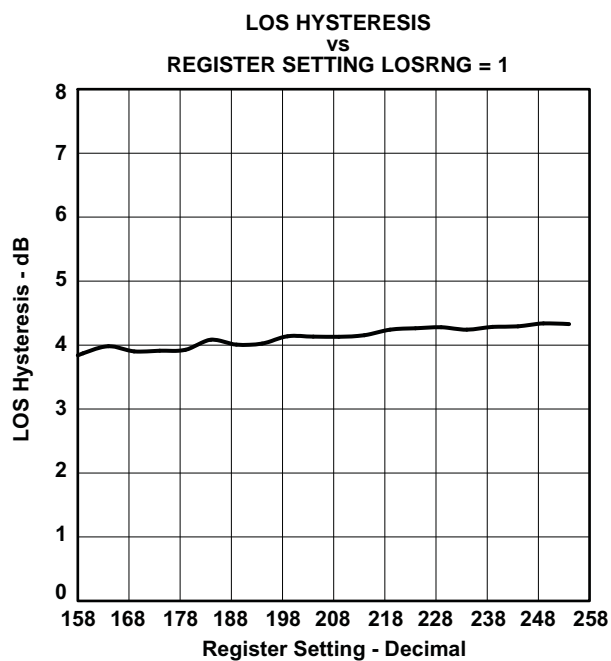


Figure 16.

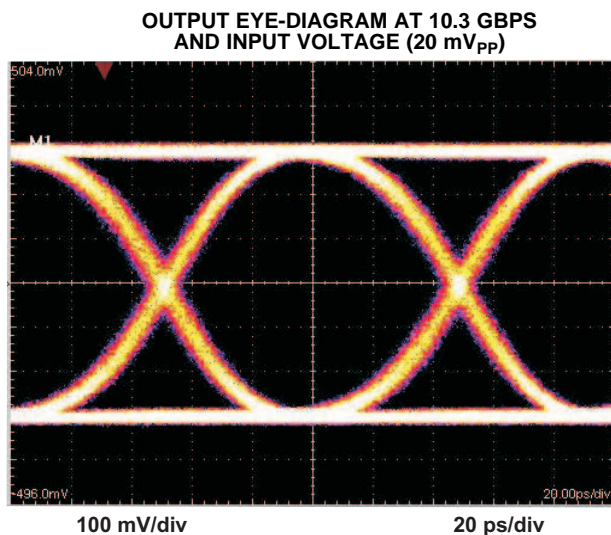


Figure 17.

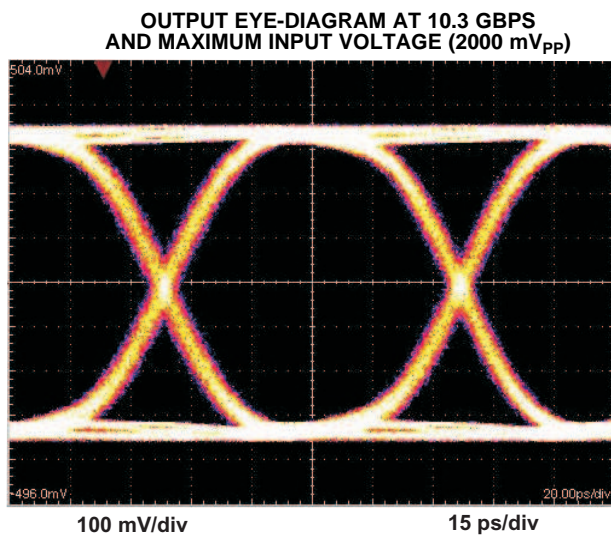


Figure 18.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted.

**OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND INPUT VOLTAGE (20 mV_{PP})**

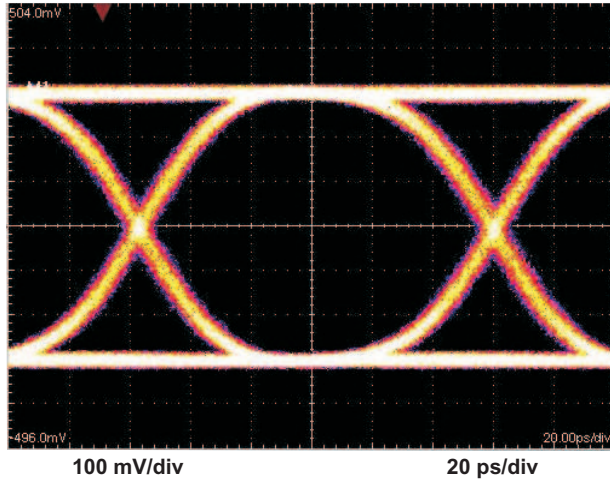


Figure 19.

**OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND MAXIMUM INPUT VOLTAGE (2000 mV_{PP})**

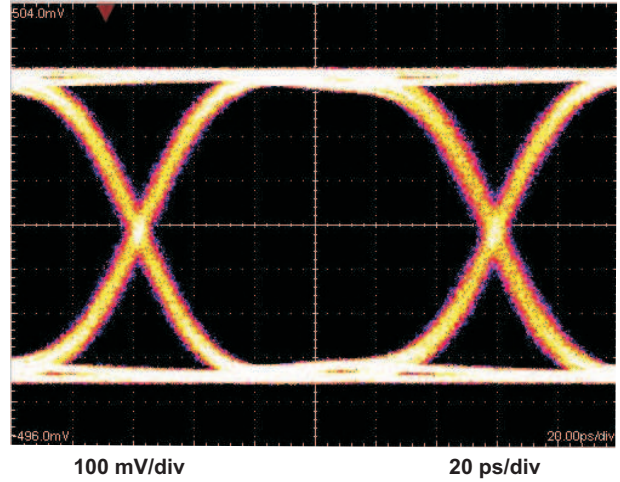


Figure 20.

APPLICATION INFORMATION

Figure 21 shows a typical application circuit using the ONET8501PB.

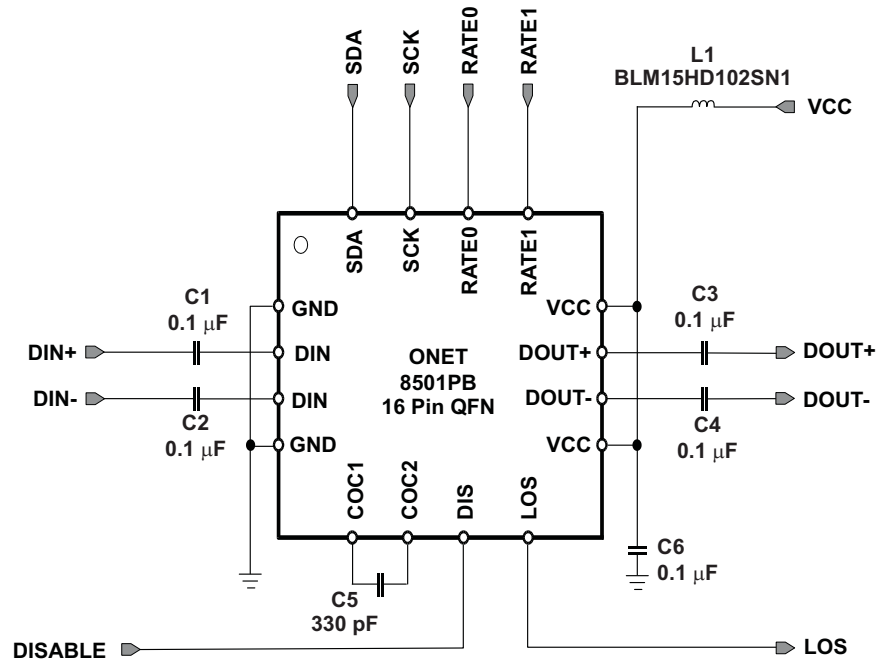


Figure 21. Typical Application Circuit

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|--------------------------------------|
| ONET8501PBRGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| ONET8501PBRGTRG4 | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| ONET8501PBRGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| ONET8501PBRGTTG4 | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

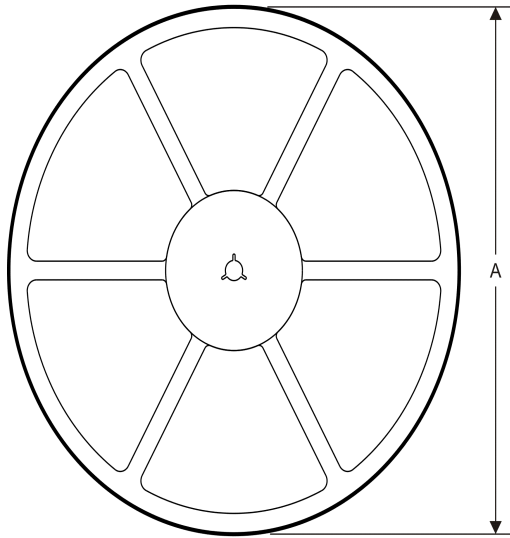
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ONET8501PBRGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| ONET8501PBRGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| ONET8501PBRGTT | QFN | RGT | 16 | 250 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

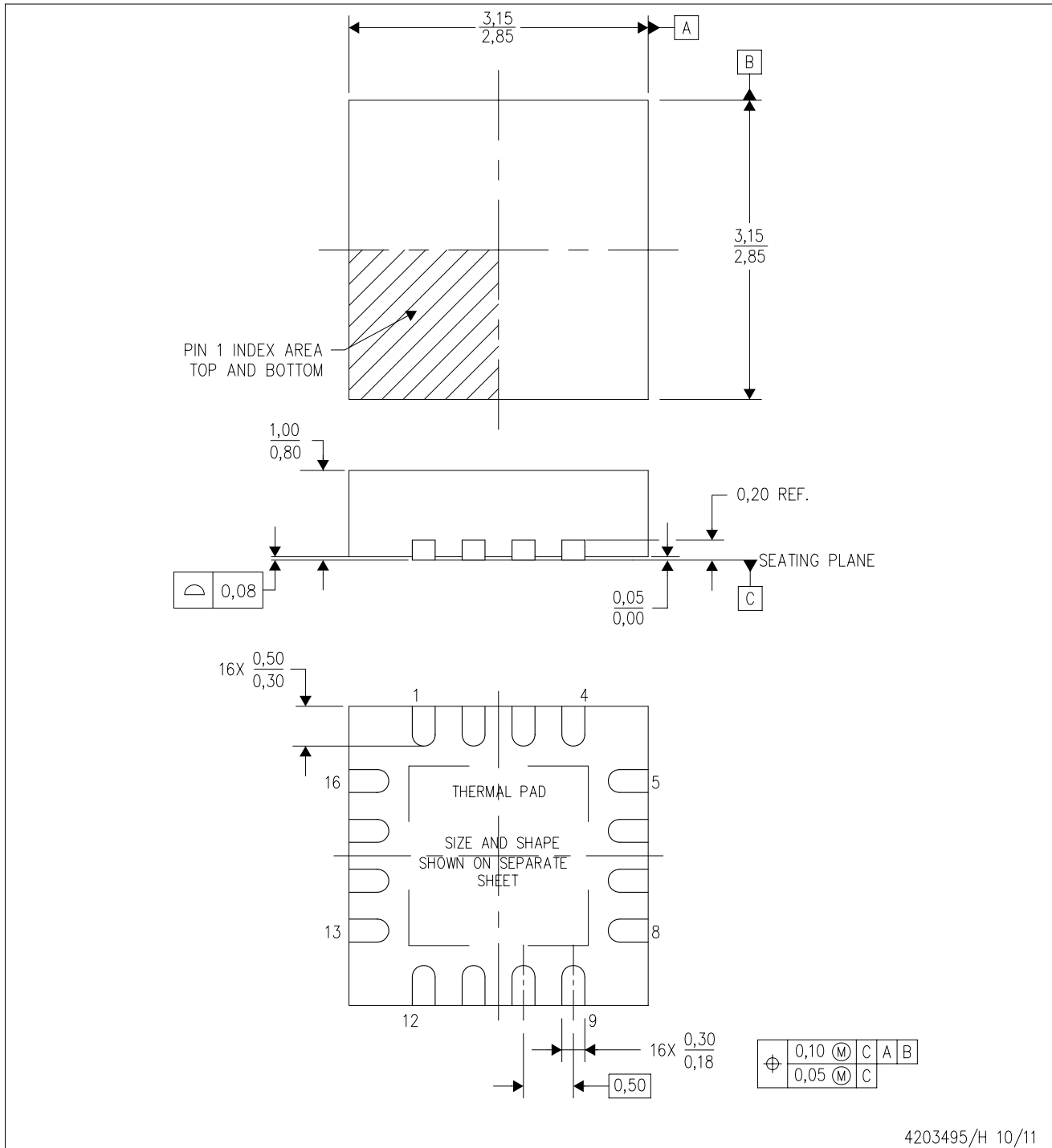
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ONET8501PBRGTR | QFN | RGT | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| ONET8501PBRGTT | QFN | RGT | 16 | 250 | 210.0 | 185.0 | 35.0 |
| ONET8501PBRGTT | QFN | RGT | 16 | 250 | 338.1 | 338.1 | 20.6 |

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

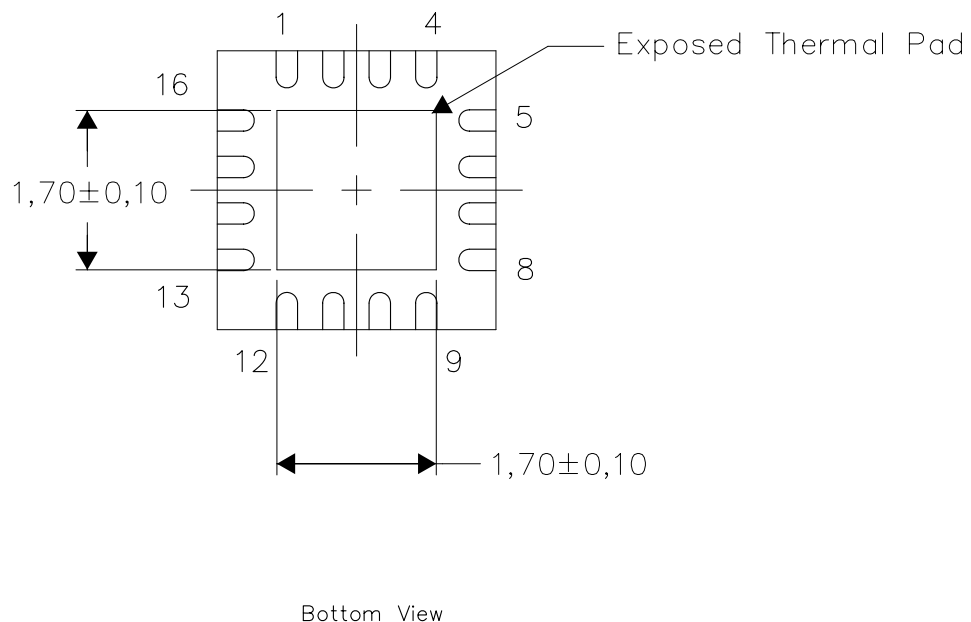
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206349-4/Q 10/11

NOTE: All linear dimensions are in millimeters

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

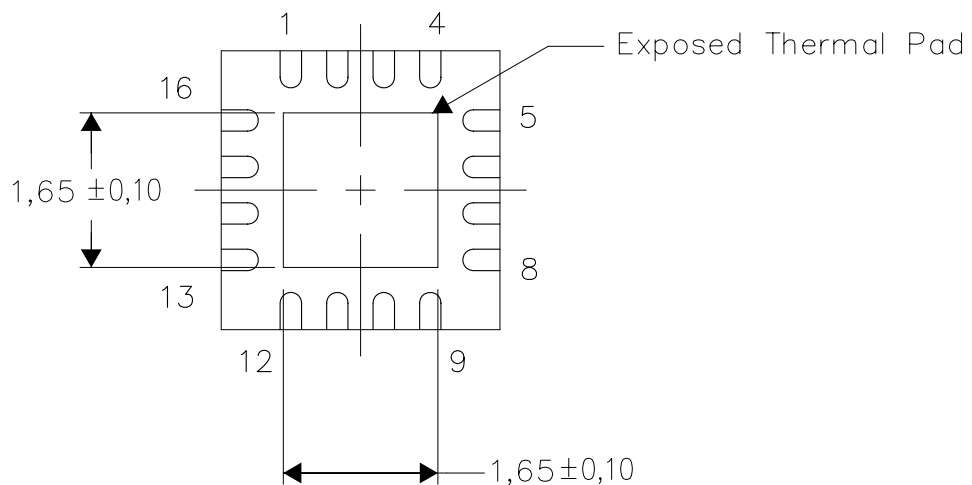
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349-7/Q 10/11

NOTE: All linear dimensions are in millimeters

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